

MIO user manual

THE STANDARD OF
EXCELLENCE IN
MICROCOMPUTER
SYSTEMS

IMSAI

CUSTOMER SERVICE

REPLACEMENT PARTS

If you need a replacement part, use only standard parts from commercial sources. Use of surplus or second-run parts will void warranty. If you have trouble locating a part, write IMSAI and include:

- Part number and description as shown in the parts list.
- Serial number of cabinet or board name and revision number.
- Date of purchase.
- Nature of defect.

Note: Parts damaged through carelessness or misuse will not be replaced under warranty.

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Need help with your kit or system?

We encourage you to call or write IMSAI for assistance with any technical problems (except program debugging and "customizing" of hardware for special application, which we will not handle).

The effectiveness of our technical assistance depends on the information you furnish. Be sure to include:

- Serial number of cabinet and/or board name and revision number.
- Date of purchase.
- Exact description of problem.
- Everything you have done in attempting to correct the problem.
- All switch positions, connections to other equipment, system configuration, operation procedure, voltage readings and any other information that you think might be useful.

Note: Telephone traffic is lightest at midweek . . . please be sure your manual and all notes are on hand at time of call.

REPAIR SERVICE

Service facilities are available for both warranty and non-warranty repair work. If this service is desired, send IMSAI:

- Name and address.
- Date of purchase.
- Copies of all correspondence and notes relevant to the problem.
- A complete description of the problem.
- Authorization to return your kit C.O.D. for service (IF ANY) and shipping charges.
- The equipment to be repaired should be sent to IMSAI well packed.
- The original packing slip number.

ERRATA INFORMATION

Errata information will be found immediately preceding the section to which the information applies and should be used for clarification and/or correction of the section indicated.

CAUTION: FAILURE TO OBSERVE PERTINENT INFORMATION WHICH IS INCLUDED WILL VOID WARRANTY.

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MIO

FUNCTIONAL DESCRIPTION

INPUT/OUTPUT VERSATILITY

The MIO, Multiple Input Output Board, is designed to meet all Input/Output requirements of most 8080 System Users by providing the User with the following Input/Output interfaces:

1. one Data Storage interface to a standard audio cassette recorder;
2. two Parallel Input/Output (PIO) ports;
3. one Serial Input/Output port; and
4. one control port to be used for internal and external control functions.

As an example of its versatility, a single MIO Board could control a TV Typewriter, a Line Printer, a Teletype, and a cassette recorder.

SOFTWARE COMPATIBILITY

Board Addressing and Port Configuration capabilities allow the MIO Board to be Address Compatible with virtually all Software Packages.

The Board is jumper selectable to any one of the 64 groups of 4 Input/Output addresses available with the 8080. Jumper selection further allows each port to be configured in any order within the selected group of 4 addresses.

As an example, a TV Typewriter, which is a parallel I/O device, may be used with serial I/O software simply by configuring the MIO Board so that the parallel port for the TV Typewriter appears at the I/O address where the serial data

normally appears.

EXTERNAL CONNECTIONS

External Interface Connections are made from the three 26-pin edge connectors at the top of the board. These contain the signals necessary for two identical parallel interfaces, and a serial I/O interface. The Current Loop or EIA options are normally configured to provide a standard EIA Data Transmission pinout at the connector.

INTERRUPT CAPABILITIES

Any of the Status Signals from each of the I/O Ports may be used to generate Interrupts. Provision is made for jumpering these Status Signals to Vectored Interrupt Lines, if a PIC-8 Board is present. They may be directly jumpered to the CPU Interrupt Line for a single level Interrupt System.

SERIAL INPUT/OUTPUT PORT

The MIO Board provides for one complete Serial I/O port which is designed to require no initialization on power-up.

BOARD OPTIONS

A number of options are available and are easily selected by the User.

1. The Baud Rate is jumper selectable and can range from 45.5 to 9600 Baud.
2. Character Length, Parity Enable, and Even/Odd Parity selection are jumper selectable.

3. The Data output of the UART may be jumpered to an EIA Driver, a Current Loop Driver, or a TTL Driver.

Similarly, the Data input of the UART may be jumpered to an EIA Receiver, a Current Loop Receiver, or a TTL Receiver.

4. Provision is made to monitor any of the UART Status Signals using the Control Input Port, or the interrupt inputs,

STATUS SIGNALS

The SIO Status Signals provided are as follows: TRANSMIT READY, the negation of TRANSMIT READY, RECEIVE READY, the negation of RECEIVE READY, PARITY ERROR, OVERRUN ERROR, and FRAMING ERROR.

An additional Status Signal, SIOS, is provided to assist in error checking routines. This signal simply indicates that one of three error conditions has occurred, (PE, FE, or OE). It may be decoded via the Control Port to determine which of the three signals is active. This feature is provided to allow efficient use of the Control Port in a case where the complete board configuration is being used.

EXTERNAL INTERFACE CONNECTIONS

The SIO Port has available at a 26 pin edge connector, all signals necessary for Standard EIA, Current Loop and TTL Serial Interfaces.

PARALLEL INPUT/OUTPUT PORTS

The MIO Board provides for 2 identical 8 bit parallel input/output ports.

BOARD OPTIONS

Board options allow the User to:

1. Use one of four types of Input Strokes: 1. positive edge, 2. negative

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edge, 3. positive level, and 4. negative level. It is also possible to continuously gate data into the latch.

2. Use PIO Status Signals to generate Interrupts or to be simply monitored by the Program via the Control Port.

STATUS SIGNALS

The PIO Status Signals which are provided are as follows:

ODR- one Output Data Ready line for each Parallel Output Port;

IDA- one Input Data Accepted line for each Parallel Input Port.

As with the SIO Port, an additional signal, PIOS, is provided to enhance the efficiency of the Control Port Input Bits.

EXTERNAL INTERFACE CONNECTIONS

The External Interface Connections for the PIO Output Ports provide for 8 Output Data Lines and 3 Control/Handshake Lines.

Each Input Port provides for 8 Input Data Lines and 2 Control/Handshake Lines.

All signals are available at two identical 26 pin edge connectors for easy interfacing to external parallel I/O devices.

CASSETTE INPUT/OUTPUT PORT

The MIO Board provides for one complete Cassette Recorder Interface.

BOARD OPTIONS

Board Options allow the User to:

1. Vary the recording rate from 500 to 62,500 bits per second.
2. Set the ^{polarity} phase of the recorded signal to provide compatibility with most all audio cassette recorders.

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The CRI Port writes Biphase Encoded Data to the tape. This can be used to generate Byte/Lancaster or Tarbell data formats.

The Biphase encoding generates Byte/Lancaster data formats by sending alternating 1's and 0's when a zero bit is to be recorded. It sends all 1's when a one bit is to be recorded. In this standard, the maximum data rate is 30 bytes per second.

The CRI can also operate in the Tarbell Standard, using one bit of phase encoding per data bit. This standard allows the User to record data at the standard rate of 187 bytes per second or faster if the recorder used is of sufficient quality.

The recorder section can have two cassette recorders connected to it at one time, thus providing the User with the basic capability for a cassette operating system.

*Tarbell Format Preferred Rate
1689 B/s*

MIO SPECIFICATIONS

Basic Configuration

1. The MIO board uses four I/O ports and is available with the following I/O interfaces:
 - Two parallel (PIO) ports
 - One control (CTL) port
 - One cassette recorder (CRI) port
 - One serial (SIO) port
2. There are three 26 pin edge connectors on the top of the board, two for the PIO ports and one for the SIO port. The SIO pin assignments are compatible with the standard EIA connectors. The PIO input pin numbers are the same as the PIO 4 port 0 input pin numbers, and the PIO output pin numbers are the same as the PIO 4 port 1 output pin numbers.
3. The board address (one of the 64 possible groups of four I/O ports) and the order of the addressing of the four ports on the board are jumper-selectable.
4. Interrupt requests are jumper-selectable to PIC-8 and CPU lines.
5. The operation of the individual ports is as follows:
 - A) SIO
 1. Baud rate is jumper-selectable for rates of 45.5 to 9600 baud.
 2. Character length, parity enable, and even/odd parity select are jumper-selectable.
 3. Transmitted serial data is available in CTL output jumper area.
 4. Received serial data is available in the CTL input jumper area.
 5. Transmit ready (TRDY), receive ready (RRDY), parity error (PE), overrun error (OE), framing error (FE), the complements of TRDY and RRDY, and (SIOS), which can represent one of (OE), (PE), (FE) or the logical OR of the three, are all available in the CTL input jumper area.
 - B) PIO
 1. Output data is latched and available at the PIO connector.
Output Data Ready (ODR) is available at the PIO connector.
Output Data Accepted (ODA) is available at CTL IJA.

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Specifications

Data Ready (DR) is available at CRL IJA.
Clear Data Ready (CDR) is available at
the PIO connector.
Data Strobe (STB) is available at the
PIO connector.

2. Input data is accepted from the PIO
connector.
Input Data Strobe (IDS) is jumper-selec-
table for positive or negative edge
triggering, gating or disable.
Input Data Accepted (IDA) is available
at the PIO connector.
Input Data Ready is available at CTL IJA.

C) CTL

1. Bits 0-3 are latched and available in OJA.
Bit 4 = write enable for CRI
Bit 5 = read enable for CRI
Bits 6 and 7 are used to control the gener-
ation of SIOS, PIOS, CRIS and PIO port
selection.

2. Output Jumper Area (OJA) has CTL bits 0-3
and SIO transmit as inputs and has the
following possible outputs:

Four EIA drivers
One current loop driver (20 or 60 milliamp)
Two TTL drivers
Three open collector 20 milliamp, 40
volt drivers

3. Input Jumper Area (IJA) has output jumper
positions to eight data input lines, eight
interrupt request lines and the serial data
input, and has as input the SIO, PIO and
CRI status signals, as well as, four EIA
and one current loop receiver.

D) CRI

The CRI is capable of writing or reading
biphase encoded data at rates of 500 to
62,500 bits per second. It can operate
in either the "Byte/Lancaster" or "Tarbell"
recording standards. (Note: the standard
rates for "Byte/Lancaster" and "Tarbell"
operation are 2400 bps and 1500 bps, re-
spectively.) The CRI can interrupt on a bit
byte basis. It has two input and two out-
put connections for cassette interface, al-
though only one input may be operating at a
given time.

THEORY OF OPERATION

The MIO, Multiple Input/Output Board, contains all the logic required to implement two latched parallel input/output (PIO) ports, a serial I/O (SIO) port, a cassette recorder interface (CRI) port and a port for the control of the other ports or external devices. The Theory of operation will be discussed by first describing the internal data bussing of the board and then discussing each of the individual types of I/O ports. The reader should be completely familiar with the MIO User Guide prior to reading the Theory of Operation.

Internal Data Bussing

The MIO board has an internal bi-directional, ^{SIO Bus} 8-bit data bus. The output information from the 8080 back panel is gated onto the internal bus whenever SOUT is asserted. When the MIO is selected and PDBIN is asserted, data is gated from the internal bus to the 8080 back panel bus. The gating is done with 74367's to increase the current sink capability to 32 milliamps per line. Each of the individual ports on the internal bus has its own 3-state driver. All of the ports except the control port have this driver as an integral part of the latches holding the information for these ports. The control input port uses a separate 74367 to gate the data onto the internal bus.

Interrupt Generation

Interrupt generation within the board is done by gating selected signals from the input jumper area onto the vectored interrupt and/or the CPU's interrupt lines using 74LS05s.

Address Selection and Decoding

Address selection for the MIO is performed with the use of six 74LS86 gates which receive the address bits as one input, and receive as the other input a high if the selected address jumper is not present, or a ground if the jumper is present. This will cause the output of the 74LS86s to be asserted if the corresponding address bit is one and the jumper is present; or if it is a zero and the jumper is not present. The six address bits are then ANDed in the 74LS30 together with the fact that either an input or output instruction is being executed (SINP or SOUT) to indicate board selection. The select pulse is used to enable a 74LS155 decoder. The address inputs to this decoder are the two least significant address bits which are jumper selected to provide the desired addresses. The outputs of the 74LS155 consist of four REGISTER LOAD pulses and four READ ENABLES, one for each of the ports. In the case of the two parallel I/O ports, the REGISTER LOAD and READ ENABLES are both fed directly to the 8212s.

The DS2 input (to complete selection on the 8212) is controlled by bit 7 of the control register, thus providing the required multiplexing.

Serial I/O Port

The serial I/O port is implemented using a universal asynchronous receiver/transmitter chip (UART). The UART is designed to add the start and stop bits required for transmitting data and to recognize these start and stop bits when receiving data. Note that the jumper configuration for the UART consists of putting +V (Vcc through a 1K resistor) on the control load pin and either ground or +V on the other select pins. The setting of the options pins is discussed in the MIO User Guide.

Parallel I/O Ports

PIO Output Ports

The two parallel input and output ports use the 8212 chips for holding and receiving data. Note again that the most significant bit of the control register is used to determine whether port 1 or port 2 is selected via the DS2 select input pin. When the REGISTER LOAD is executed, the data is loaded during /PWR. The 8212 is deselected on the trailing edge of /PWR which causes the interrupt line (Pin 23) to go high on the 8212. This signal is used as a DATA READY output signal for the port. When the output system has accepted the data, it responds by sending a positive pulse (CLEAR OUTPUT DATA READY) on the strobe input. This causes the interrupt line in the 8212 to be cleared thus indicating that the external interface is ready for more parallel data.

PIO Input Ports

The strobe input from the external device first goes through an EXCLUSIVE OR gate. A jumper to this gate is used to sense a positive strobe, while the absence of a jumper is used for a negative strobe. The LOAD one shots are triggered on the high-to-low transition on the output of the 74LS86's. The second jumper area selects the input strobe, or the LOAD one shot, to gate the data into the 8212 and to set the interrupt line (Pin 23) low thus indicating that input data is ready. If no jumper is used, the input data is continuously available to the 8080. When the 8212 register is read by the computer, the 8212 being selected will cause the interrupt line to reset, indicating to the external system that the data has been accepted, and removing the ready pulse internally.

Control Port

The control register output consists of two 74LS175s; one of which is used to hold the four least significant bits of the data for use in the output jumper area and the other of which is used to hold the four most significant bits for controlling the internal operation.

The internal operations use bit 4 asserted to indicate that a write operation is being performed on the CRI and bit 5 to indicate that a read operation is being performed on the CRI. Bits 6 and 7 are used in two different modes: 1) to select the status input lines for SIOS and PIOS by providing the A and B inputs to the 74LS153 dual 4 to 1 selector; and 2) to multiplex the PIO select lines and the status signal, CRIS. Bit 7 is used to multiplex the PIO ports by having /CR7 as the DS2 input to the 8212s for PIO-Port 1; and CR7 as the DS2 input to the 8212s for PIO Port 2. Bit 6 is used to select the Byte Ready (/CR6) or Bit Ready (CR6) signal for input to the CRIS signal.

The input to the control port is accomplished by selecting the appropriate jumpers in the input area as described in the User Guide. These jumpered inputs are input to the 74LS367s for gating onto the internal data bus.

Cassette Recorder Interface

The Cassette Recorder interface uses the ANSI standard bi-phase encoding technique to record data on the tape by using a square wave clock to shift the data and EXCLUSIVE ORing the clock with the output data.

Timing

Figure 1 shows a timing illustration of how the CRI interface works with respect to shifting, recording, and recovering the data. The top line shows the serial data which is to be written on the tape. Below this is the clock pulse. The third line shows the serialized data as clocked out of U36. The fourth line shows EXCLUSIVE OR of the clock and the data. Notice that there are two flux reversals or one complete cycle per bit when a constant data stream is being written and only one flux reversal or one cycle per two bits when alternating ones and zeros are being written. The fifth line shows the EXCLUSIVE OR of the data and the inverted clock. The sixth line shows the resultant sinusoidal wave form which is written on the tape. This can also be considered to be the data read directly back from the tape. The seventh line shows the output of the 8T20

which is a digital form of the received data. Line 8 shows the output of the zero crossing one-shot detector as if it were never disabled. Line 9 shows the disable gate for this zero crossing detector. This is the output of the 74LS74 flip-flop. Line 10 shows bit 4 coming high in the counter. The leading edge of bit 4 is used to strobe the data on the return. Line 11 shows the reconstructed data stream.

The reader should become familiar with the diagram before proceeding on with the discussion. Notice that the polarity of the written data and/or the digital recovered data output of the 8T20 can be inverted when it goes through the EXCLUSIVE OR gates. Switches 7 and 8 in the External Address Jumper are used to invert the output and input data, respectively. This option is provided so that the proper data will be fed into your recorder and returned from it independently of the phase on which the recorder operates.

Pin 1 of the 8T20 fed back through R44 provides the hysteresis for the 8T20. The given value of R44 works with most popular recorders. If adjustment should be necessary, its value should be lowered to increase the hysteresis and raised to decrease it.

The shift register used in this section is a 74LS395. This provides both the tri-state outputs for gating onto the internal data bus and the cascadeable output for forming an 8-bit shift register. The timing generator consists of the two 74LS163s and the 74LS293. The 74LS163s should be jumper-selected so that they reload at sixteen times the required data frequency. The 74LS293 divides down the output of the 74LS163s to generate timing for the read and write circuitry.

Cassette Read Operation

In read operation, the first transition received from the recorder starts the CRI clock. After four clock cycles, the eight-bit shift register is clocked, loading the current level of the input data into the register. After twelve clock cycles, the 74LS293 is put into reset, and the 74LS163s are put into LOAD mode, thus presetting and holding them. The entire circuit then idles until the next input transition, which again allows the counters to run.

Referring again to Figure 1, line 8 (labelled zero crossing), represents the output of the 8T20 one shot as if it were never disabled. That is, it generates a short pulse for every zero-crossing transition input from the recorder. The one-shot disable flip-flop (U36), however, prevents the one-shot from detecting a transition from the time the first transition starts the counters until the twelfth clock cycle, when the clocks are disabled.

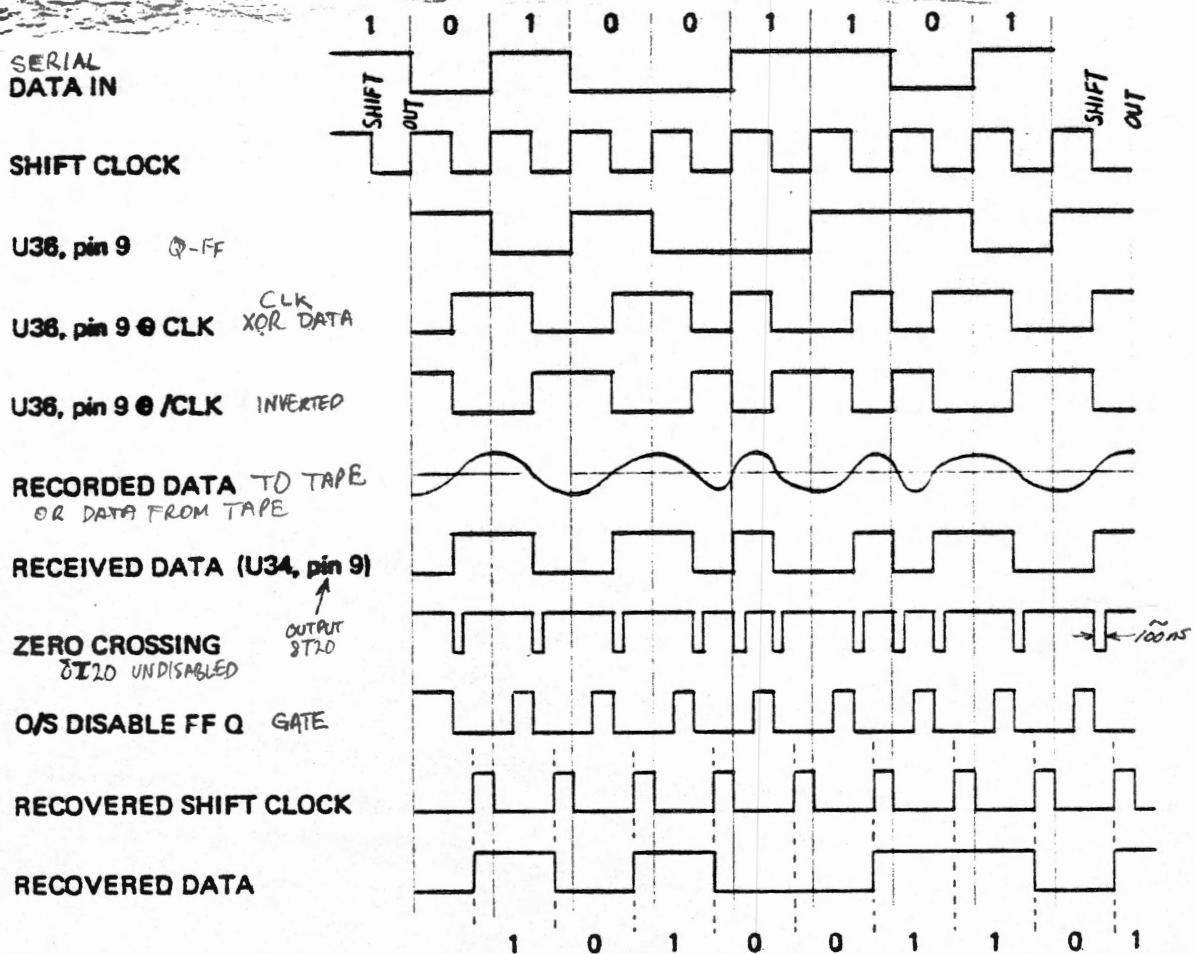
In the input data stream from the recorder, when the present data bit is the same as the previous data bit, a second transition occurs at approximately the eighth clock cycle. Because the one-shot is disabled, this transition will not be detected. However, the next transition will occur after the twelfth clock cycle, enabling the counters, and causing the data level to be read four clock cycles later, as described above.

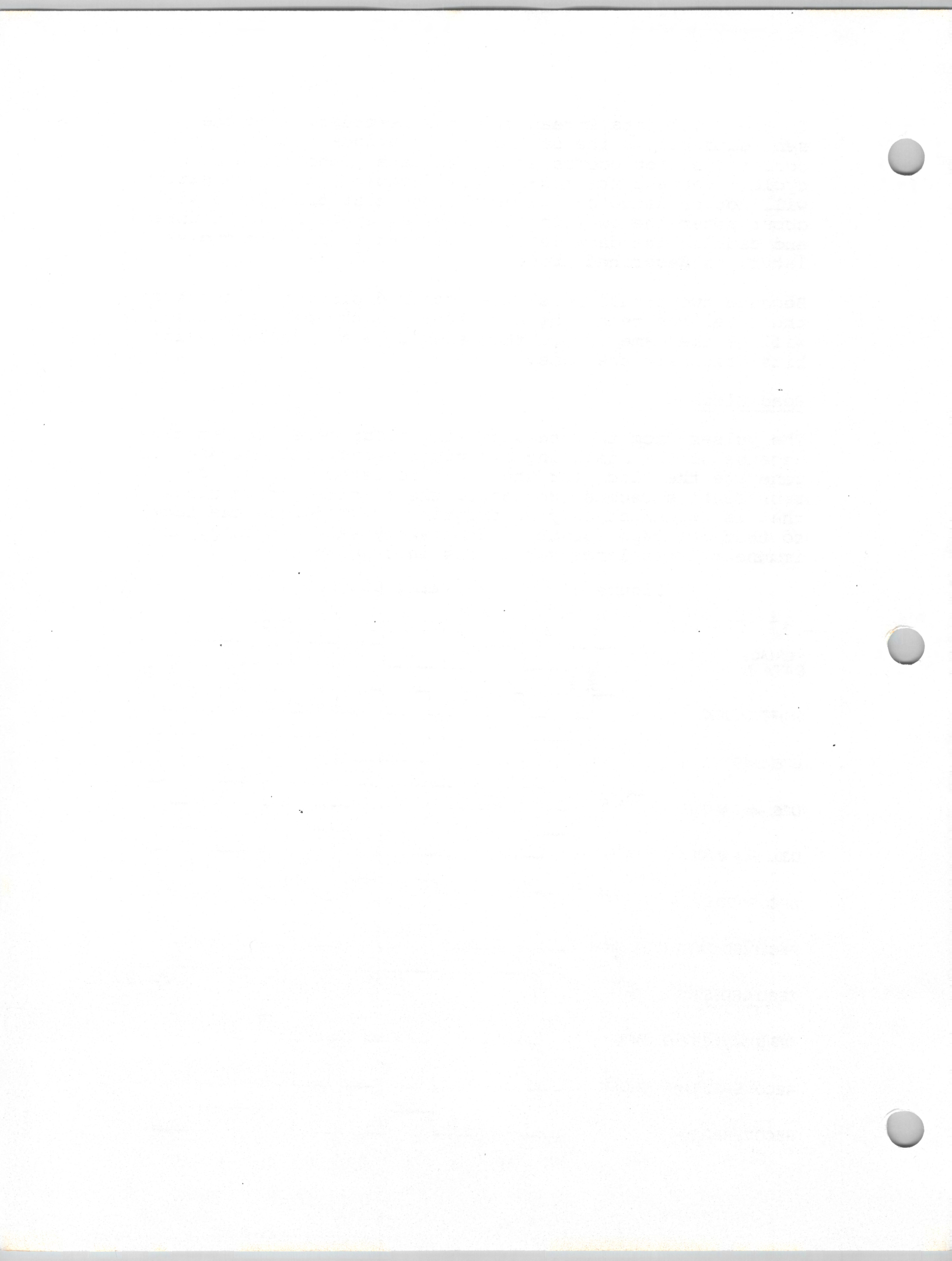
Because two transitions have occurred since the last time the level was read, the new level and the previous level will be the same, which they should be to represent data bits which are the same.

Read Clock

The pulses from the one-shot will occur once per bit time because of the disabling described above, and are used to generate the clock for the shift register. This clock represents a reconstruction of the original write clock, one that is dependent only on transitions read from the tape, so that the tape format is inherently self-clocking, and immune to even large variations in tape speed.

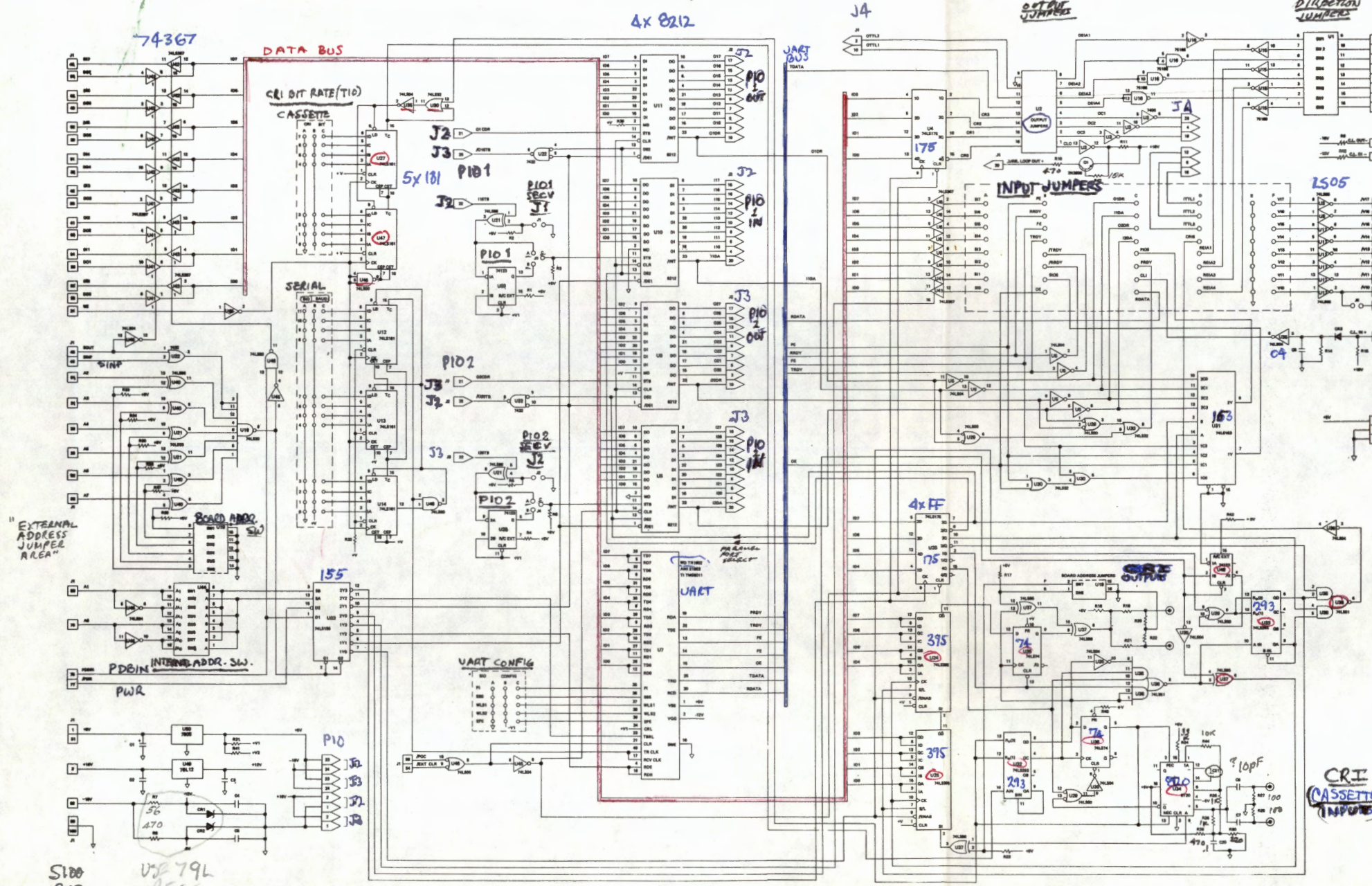
Figure 1 Timing Diagram





REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL	11/76	
1	ECN 77-0012, 77-0004	2/77	
2	ENC 77-0002	5/77	

J2 - PIO 1
 J3 - PIO 2
 J4 - SIO →



U1	DIRECTION JUMPERS	C1	33uF
U2	OUTPUT JUMPERS	C2	.1uF
U3	7406	C3	
U4	74LS175	C4	.02uF
U5	74LS04	C5	
U6	74367	C6	
U7	UART 1602A ✓	C7	thru .1uF
U8		C8	
U9		C20	
U10	8212	R1	36K 1/4w
U11		R2	1K 1/4w
U12		R3	
U13	74LS163 or 74LS161	R4	36K 1/4w
U14		R5	1K 1/4w
U15	75189 1489	R6	
U16	75188 1488	R7	56 1/4w
U17	74LS05	R8	470 1/4w
U18	74LS30	R9	1.2K 1/4w
U19	BOARD ADDRESS JUMPERS	R10	470 1/4w
U21	74LS86	R11	10K 1/4w
U22	7432 - LS	R12	470 1/4w
U23	74LS155	R14	330 1/4w
U24	74LS395	R15	1.2K 1/4w
U25		R17	1K 1/4w
U26	74LS175	R18	1K 1/4w
U27	74LS163 or 74LS161	R19	10K 1/4w
U29	74LS00	R20	1K 1/4w
U30	74LS32	R21	10K 1/4w
U31	74LS153 or 253	R22	1K 1/4w
U32	74LS293	R23	1K 1/4w
U33		R24	36K 1/4w
U34	8T20	R25	1K 1/4w
U35	74LS04	R26	100 1/4w
U36	74LS74	R27	470 1/4w
U37	74LS86	R29	470 1/4w
U38	74LS51	R30	220 1/4w
U39	74LS123 or 74123	R31	
U40	74LS86	R41	thru 1K 1/4w
U41	(LS)	R42	10K 1/4w
U42	74367	R43	36K 1/4w
U43		R44	10K 1/4w
U44	INTERNAL ADDRESS JUMPERS	CR1	1N4742
U45	74LS04	CR2	1N751A
U46	74LS00	CR3	1N914
U47	74LS161 or 74LS163	Q1	2N3906
U48	74LS123 or 74123		
U49	78L12		
U50	7805		

CASSETTE

CRT CASSETTE INPUT

UN = CASSETTE CKT

TOLERANCES UNLESS OTHERWISE SPECIFIED		© 1977 IMSAI MFG. CORP., SAN LEANDRO, CA. ALL RIGHTS RESERVED WORLDWIDE MADE IN U.S.A.	
FRACTIONS DEC.	ANGLES	MIO REV. 2 11/76 SCHEMATIC DIAGRAM	
±	±	APPROVALS	DATE
DRAWN		CHECKED	
SCALE	SIZE	DRAWING NO.	
	B		
DO NOT SCALE DRAWING		SHEET	

NOTE: AUGAT PINS NOT SHOWN

PIO STROBE

BOARD ADDRESS
STROBE EDGE

UART
CONF.

INPUT
JMPR
AREA

OUT J.

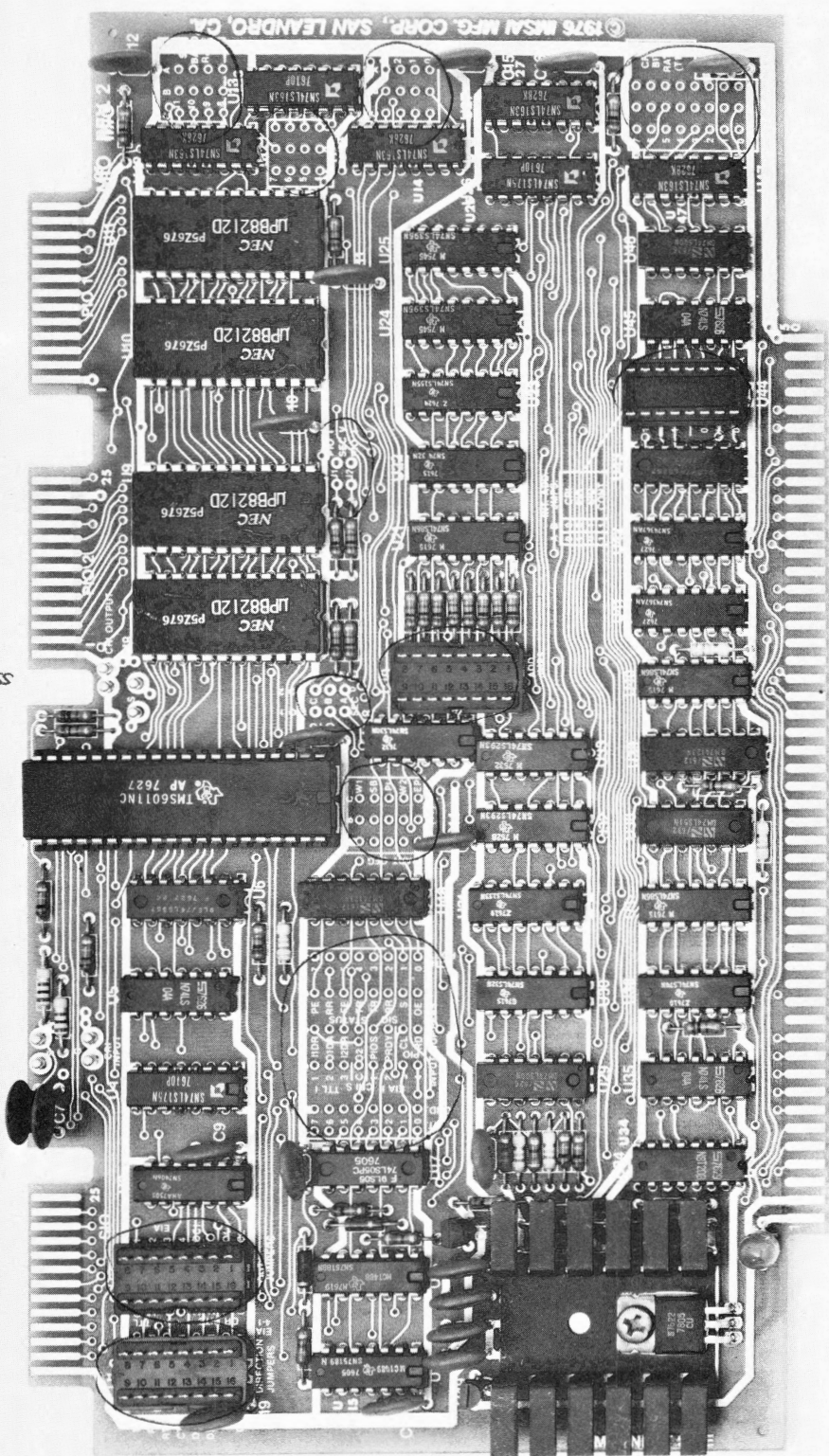
DIR J.

SIO BAUD

" "

" "

CRI BIT RATE

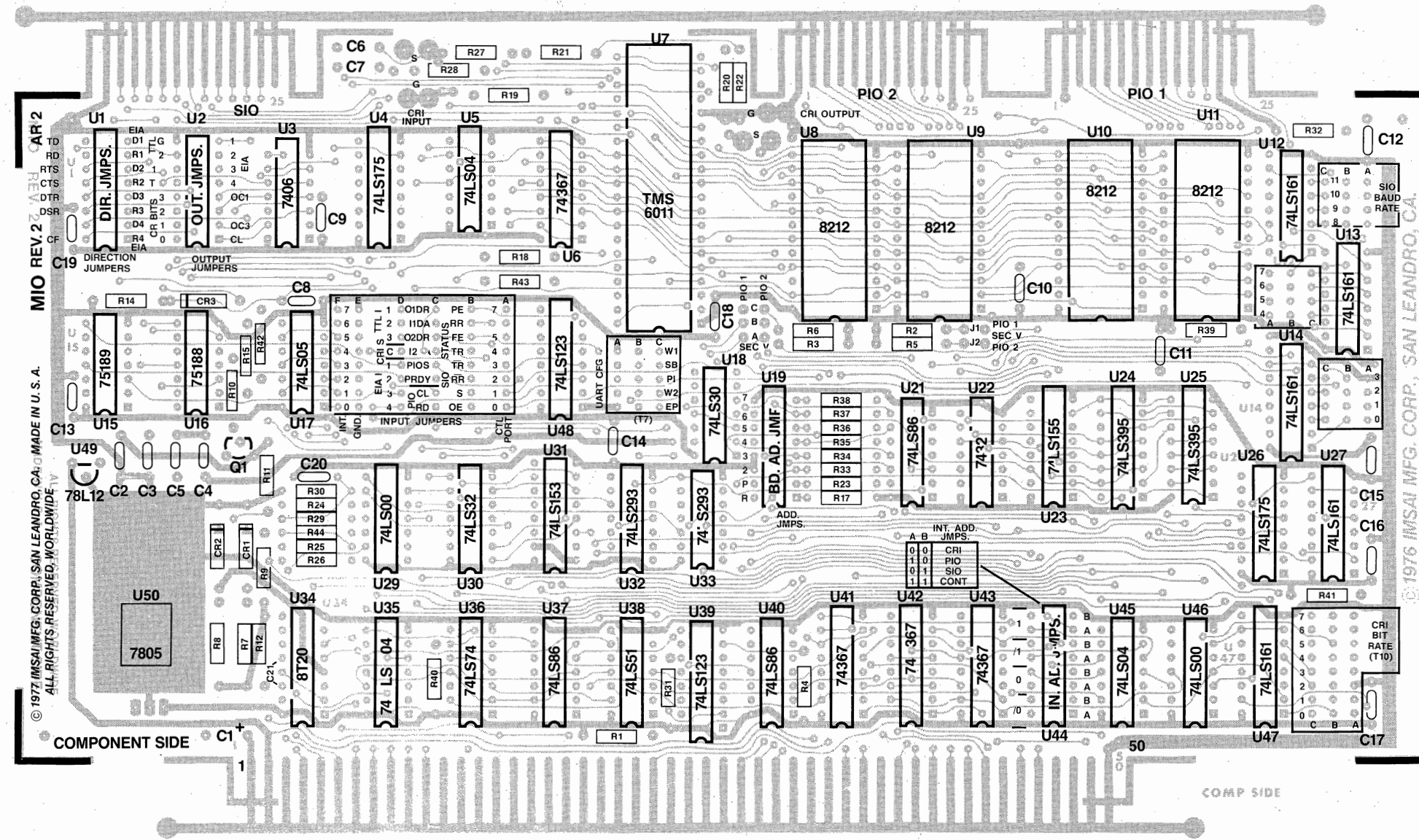


INTERNAL ADDRESS

MIO REV. 2

NON-VECT
INTERUPT

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL MIO REV. 2	11/76	ajk
1	ECN 77-0012, 77-0004	2/77	
2	ECN 77-0062	5/77	



NOTES:
 U1, U2, U19 & U44 are with 16 pin sockets.
 U7 is a TMS 6011.
 U12, U13, U14, U27 & U47 are 74LS161 or 74LS163.
 U39 & U48 are 74LS123 or 74123.
 Capacitors are .1uF unless noted below.
 C1 is 33uF.
 C6 & C7 are .02uF.
 C21 is 10 pF. C21 is on circuit side of board.
 Resistors are 1/4 watt unless noted.
 R1, R4, R24 & R43 are 36K.
 R2, R3, R5, R6, R17, R18, R23, R25, R26 & R31 through R41 are 1K.
 R7 is 56 1/2 watt.
 R8 is 470 1/2 watt.
 R9 & R15 are 1.2K.
 R10, R12 & R29 are 470.
 R11, R19, R21, R42 & R44 are 10K.
 R14 is 330.
 R27 & R28 are 100.
 R30 is 220.
 Diode CR1 is 1N4742.
 Diode CR2 is 1N751A.
 Diode CR3 is 1N914.
 Transistor Q1 is 2N3906.

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TOLERANCES UNLESS OTHERWISE SPECIFIED		FRACTIONS DEC.		ANGLES		± ± ±	
APPROVALS		DATE		© 1977 IMSAI MFG. CORP., SAN LEANDRO, CA. ADD © 1977			
DRAWN <i>DMW</i>		11/10/76		MIO REV. 2 11/76 ASSEMBLY DIAGRAM			
CHECKED <i>JA</i>		11/12/76		SCALE	SIZE	DRAWING NO.	
					B		
DO NOT SCALE DRAWING						SHEET	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL	11/24/76	

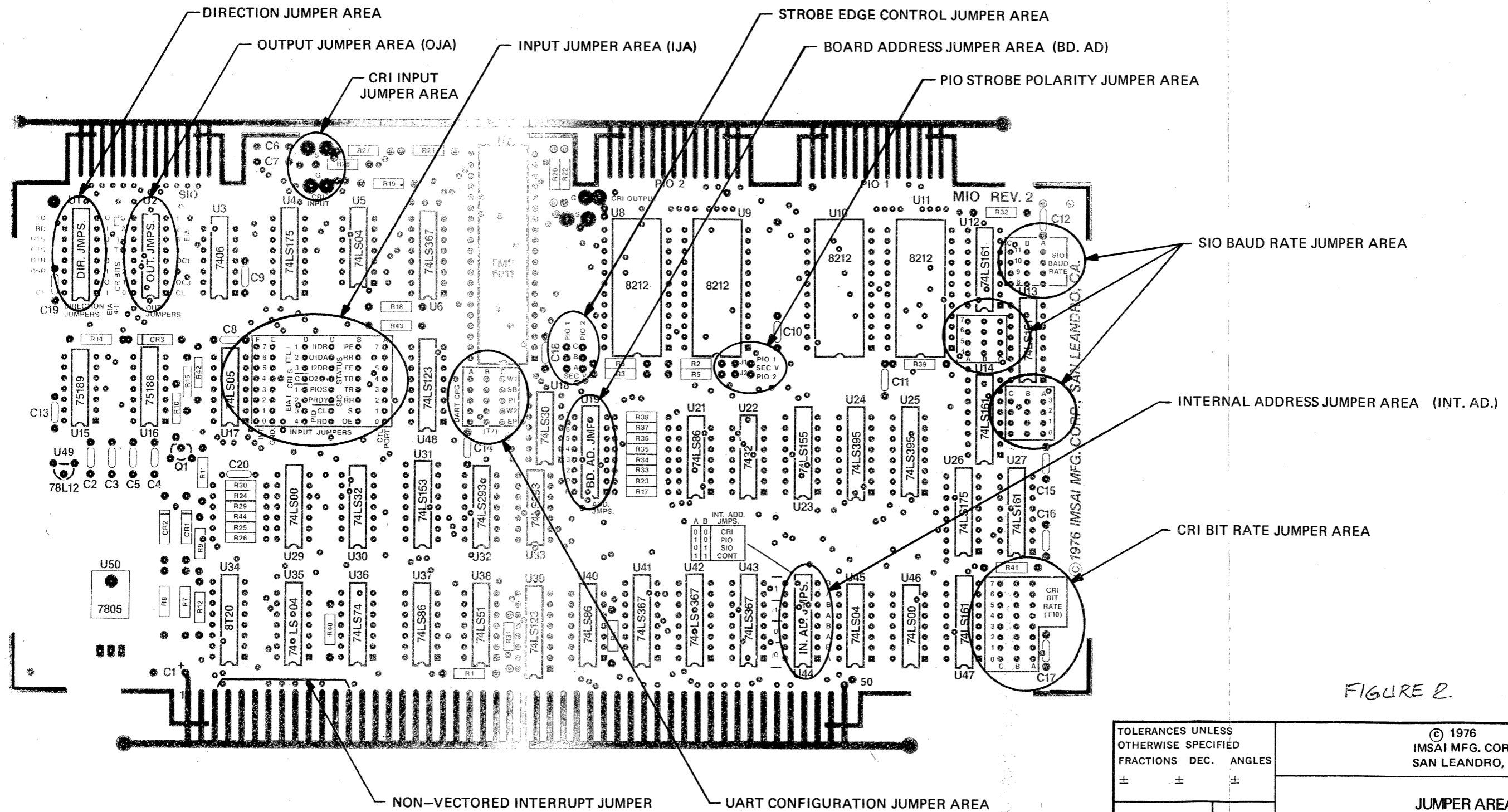


FIGURE 2.

TOLERANCES UNLESS OTHERWISE SPECIFIED		© 1976 IMSAI MFG. CORP. SAN LEANDRO, CA.	
FRACTIONS	DEC.		
±	±	±	JUMPER AREA MAP MIO REV. 2
APPROVALS	DATE	SCALE	
DRAWN <i>C. DeLo</i>	11/17/76	SIZE B	
CHECKED		DRAWING NO.	
DO NOT SCALE DRAWING			SHEET

MIO
Parts List

BOARD: MIO Rev. 2

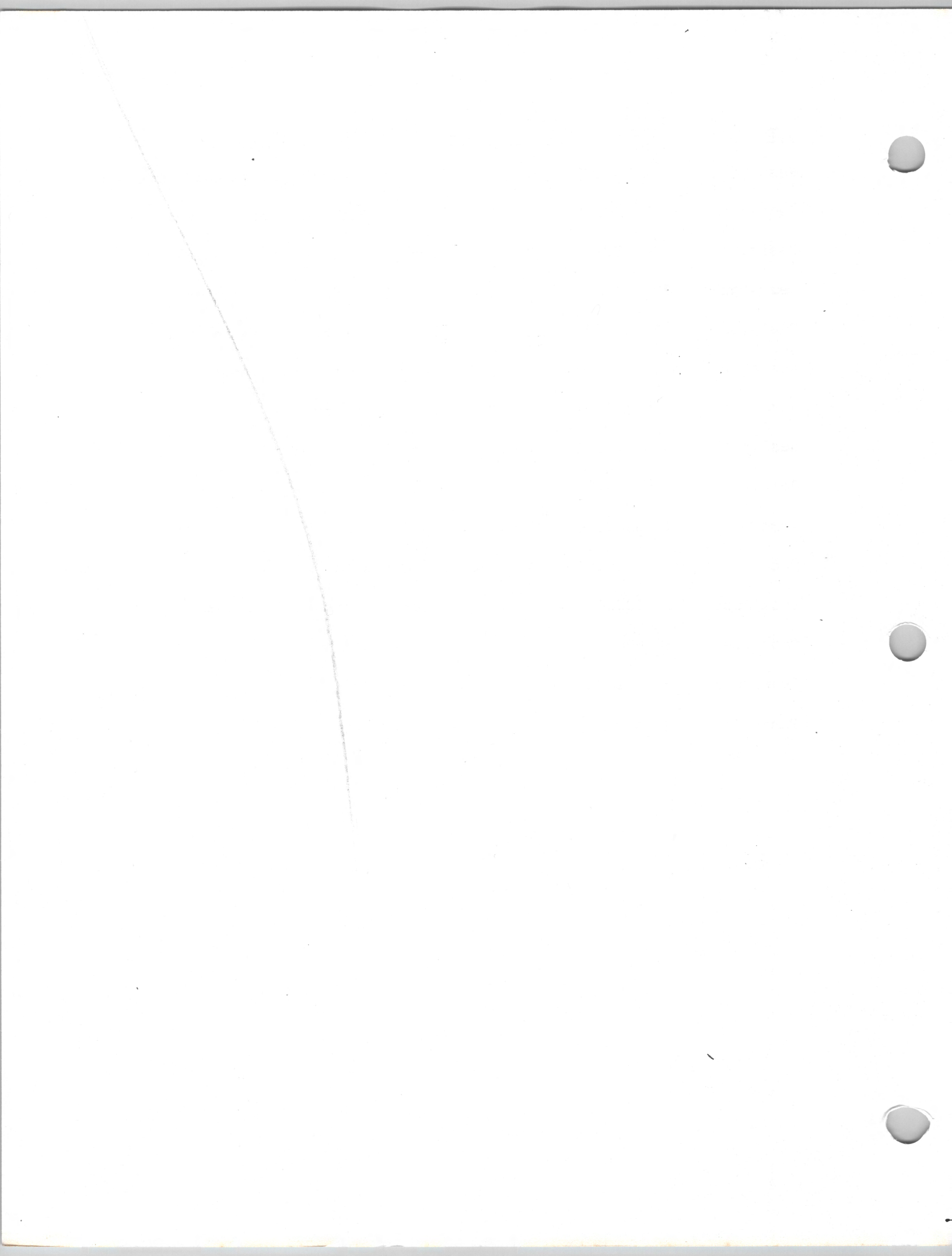
<u>ITEM</u>	<u>IMSAI PART #</u>	<u>QUANTITY</u>	<u>DESCRIPTION/IDENTIFYING MARKS</u>
PC Board	92-0000042	1	MIO Rev. 2
74LS00	36-0740002	2	Quad 2 Input NAND (Low Power Schottky)/ SN74LS00N
74LS04	36-0740402	3	Hex Inverter (LPS)/SN74LS04N
74LS05	36-0740502	1	Hex Inverter, Open Collector (LPS)/ 74LS05PC
7406	36-0740601	1	Hex Inverter Driver, Open Collector/ SN7406N
74LS30	36-0743002	1	8 Input NAND (LPS)/SN74LS30N
7432	36-0743201	1	Quad 2 Input OR/SN7432N
74LS32	36-0743202	1	Quad 2 Input OR (LPS)/SN74LS32N
74LS51	36-0745102	1	AND-OR Inverter (LPS)/DM74LS51N
74LS74	36-0747402	1	Dual D Flip-Flop (Preset and Clear) (LPS)/SN74LS74N
74LS86	36-0748602	3	Quad 2 Input EXCLUSIVE OR (LPS)/ SN74LS86N
74LS123	36-7412302	2	Dual One Shot/SN74LS123N (Alternate 74123/DM74123N)
74LS153	36-7415302	1	Dual 1 of 4 Data Selector (LPS)/ SN74LS153
74LS155	36-7415502	1	Dual 2 of 4 Line Decoders (LPS)/ SN74LS155N
74LS161	36-7416102	5	4 Bit Counter, Binary Asynchronous Clear (LPS)/SN74LS161N (Alternate 74LS163/SN74LS163N)
74LS175	36-7417502	2	Quad D Type Flip-Flop (LPS)/ 9LS/74LS175
74LS293	36-7429302	2	4 Bit Binary Counter (LPS)/74LS293PC
74367	36-7436701	4	Hex Tri-State Buffer/DM74367N

MIO
Parts List

<u>ITEM</u>	<u>IMSAI PART #</u>	<u>QUANTITY</u>	<u>DESCRIPTION/IDENTIFYING MARKS</u>
74LS395	36-7439502	2	4 Bit Shift Register with 3 State Outputs/SN74LS395N
75188=1488	36-7518801	1	RS232 Driver/SN75188N
75189=1489	36-7518901	1	RS232 Receiver/SN75189N
7805	36-0780501	1	5V Positive Regulator/7805CU
78L12	36-0781202	1	Regulator/MC78L12CP
8212	36-0821201	4	Input-Output Port/PB8212D
8T20	36-0082001	1	Bi-Directional One Shot/N8T20B
TR1602	36-0601101	1	Universal Asynchronous Receiver/Transmitter 51883/TMS 6011
1N751A	35-1000005	1	Zener Diode/1N751A 5.1V
1N914	35-1000006	1	Silicon Diode/1N914 = 4454
1N4742	35-1000009	1	Zener Diode/1N4742 12V
Transistor	35-2000003	1	2N3906 Transistor/2N3906
Capacitor	32-2010010	17	.1uF Disk Ceramic
Capacitor	32-2233070	2	33uF, 25V Tantalum
Capacitor	32-2002010	2	.02uF Disk Ceramic
Heat Sink	16-0100004	1	Thermalloy 6 Prong/6072B
Header	23-0400001	4	16 Pin IC Header
Socket Carrier	23-0900008	9	Lead Socket Carrier Assembly/AUGAT 716-AG2D
Socket	23-0800001	4	16 Pin Solder Tail IC Socket
Socket	23-0800004	1	40 Pin Solder Tail IC Socket
Resistor	30-2560462	1	56 Ohm, 1/2 Watt/green, blue, black
Resistor	30-3100362	5	100 Ohm, 1/2 Watt/brown, black, brown (3 are supplied for optional 60MA current loop.)

MIO
Parts List

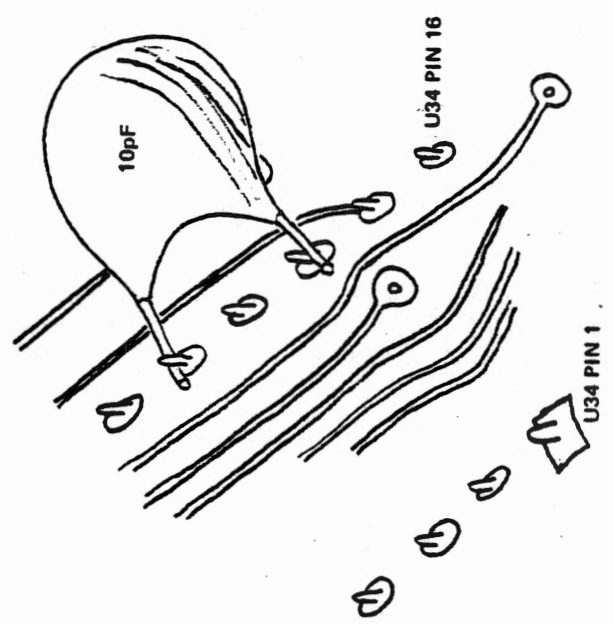
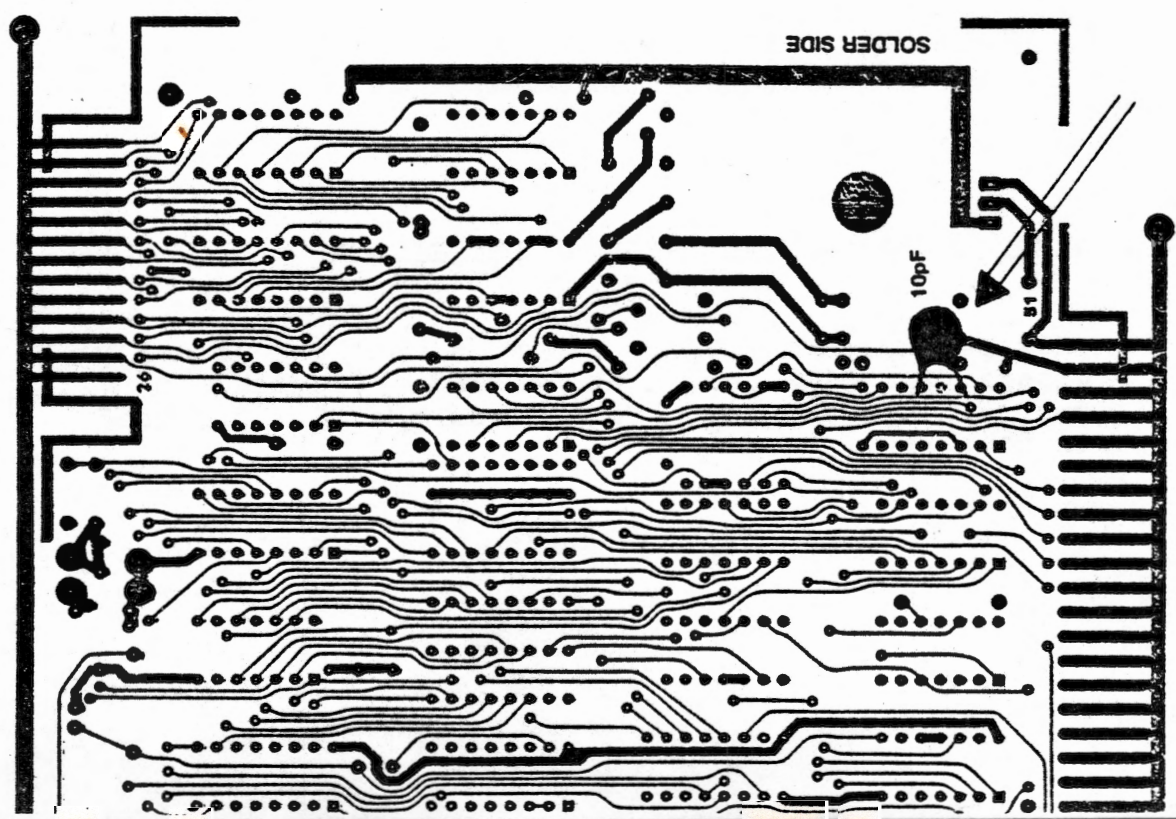
<u>ITEM</u>	<u>IMSAI PART #</u>	<u>QUANTITY</u>	<u>DESCRIPTION/IDENTIFYING MARKS</u>
Resistor	30-3330362	1	330 Ohm, 1/4 Watt/orange, orange, brown
Resistor	30-3220362	1	220 Ohm, 1/4 Watt/red, red, brown
Resistor	30-3470362	3	470 Ohm, 1/4 Watt/yellow, violet, brown
Resistor	30-3470462	1	470 Ohm, 1/4 Watt/yellow, violet, brown
Resistor	30-4100362	22	1K Ohm, 1/4 Watt/brown, black, red
Resistor	30-4120362	2	1.2K Ohm, 1/4 Watt/brown, red, red
Resistor	30-5100362	5	10K Ohm, 1/4 Watt/brown, black, orange
Resistor	30-5360362	4	36K Ohm, 1/4 Watt/orange, blue, orange
Solder	15-0000001	10'	
Screw	20-3302001	1	6-32x5/16" Phillips Pan Head Machine
Nut	21-3120001	1	6-32 CAC Hex Nut
Lockwasher	21-3350001	1	#6 Internal Tooth CAC Lockwasher
Cassette	88-0000019	1	Test Cassette
Capacitor	32-0210010	1	10pF Disk Ceramic
Pins	23-0900007	8	Cambion Socket Pins, #450-3704-01-04 (or -03 or -06)



ERRATA MIO REV.2 *DONE* 1/22/77

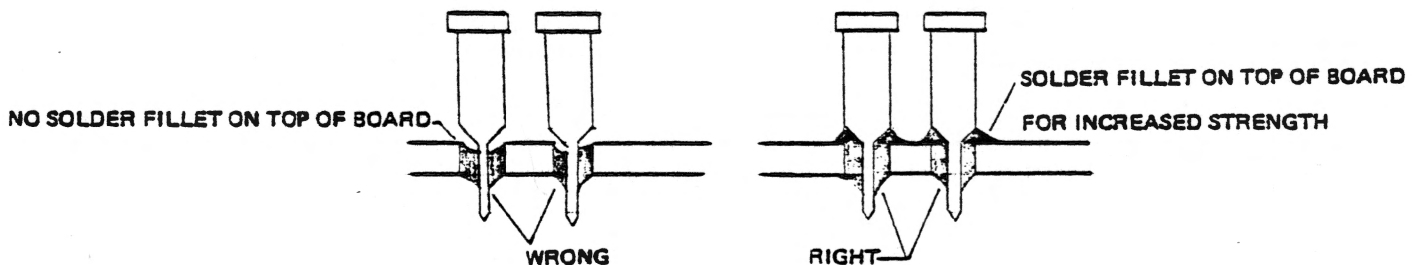
5-1-83

Board Assembly Modification to lengthen the pulse generated by the 8T20 for more reliable resetting of U36: After the board is assembled, install a 10 picofarad disk capacitor between U34 pins 12 and 14. Cut leads to 1/8" and solder to U34 pins 12 and 14 on the solder side of the board as shown. Take care not to damage the solder mask or create a solder bridge to the neighboring traces.



Assembly Note:

1. When installing socket pins for jumpers, heat should be applied long enough (e.g. 3 seconds rather than 1 second) to allow solder to wick through the board and form a fillet on the component side. (Alternately solder can be applied from the top side.) This provides greater support to the socket pins so they won't bend during jumper installation. Number 26 or 27 wire, solid, is ideal to use for jumpers. Larger wire, up to 24 solid or cut leads from $\frac{1}{4}$ Watt resistors, may be used; however, the larger wire may spring the internal contacts, requiring that you always use the larger wire. Often, leads cut from signal diodes (1N914 and 1N4148) are the ideal smaller diameter.



2. It has come to our attention that the jumpers between the Augat pins can short to other pins. This can be solved by using either some spaghetti tubing on the No. 26 bare wire or using No. 26 solid insulated wire for these jumpers. DO NOT SOLDER JUMPERS INTO THE AUGAT PINS.

ASSEMBLY DIAGRAM AND SILK SCREEN ERRATA

IC's U41 through U43 are shown on both the Assembly Diagram and Silk Screen as 74LS367. Provided in your kit are 74367's. Please use the IC's provided in your kit.

ASSEMBLY INSTRUCTIONS

- () 1. Unpack your board and check all parts against the parts list enclosed in the package.
- () 2. If gold contacts on the edge connector appear to be corroded, use pencil eraser to remove any oxidation. NOTE: Do not use Scotchbright or any abrasive material as it will remove the gold plating.

RESISTOR INSTALLATION

- (✓) 3. Insert and solder the four ^{33K}36K ohm, ½ watt (orange, blue, orange) resistors at locations R1, R4, R24, and R43 as shown on the Assembly Diagram.
- (✓) 4. Insert and solder the twenty-two 1K ohm, ½ watt (brown, black, red) resistors at locations R2, R3, R5, R6, R17, R18, R20, R22, R23, R25, R26, and R31 through R41 as shown on the Assembly Diagram. Note that the resistor at location R31 should be soldered into the +5 trace, the larger trace below the resistor. Notice that R4 and R40 are soldered into the same trace.
- (✓) 5. Insert and solder the two 1.2K ohm, ½ watt (brown, red, red,) resistors at locations R9 and R15 as shown on the Assembly Diagram.
- (✓) 6. Insert and solder the three 470 ohm, ½ watt (yellow, violet, brown) resistors at locations R10, R12, and R29 as shown on the Assembly Diagram.
- (✓) 7. Insert and solder the five 10K ohm, ½ watt (brown, black, orange) resistors at locations R11, R19, R21, R42 and R44 as shown on the Assembly Diagram.
- (✓) 8. Insert and solder the two 100 ohm, ½ watt (brown, black, brown) resistors at locations R27 and R28 as shown on the Assembly Diagram.
- (✓) 9. Insert and solder the one 220 ohm, ½ watt (red, red, brown) resistor at location R30 as shown on the Assembly Diagram.
- (✓) 10. Insert and solder the one 330 ohm, ½ watt (orange, orange, brown) resistor at location R14 as shown on the Assembly Diagram

MIO
Assembly Instructions

- RS 280
UART
8T20
70mA
-12V
10mA
-5V
- () 11. Insert and solder the one 56 ohm, $\frac{1}{2}$ watt (green, blue, black) resistor at location R7 as shown on the Assembly Diagram.
 - () 12. Insert and solder the one 470 ohm, $\frac{1}{2}$ watt (yellow, violet, brown) resistor at location R8 as shown on the Assembly Diagram.

IC INSTALLATION

All Pin 1's are toward the lower right hand edge of the PC board and the 100 pin connector. The pads for Pin 1 are square.

- () 13. Insert and solder the one 7406 at location U3 as shown on the Assembly Diagram.
- () 14. Insert and solder the two 74LS175's at locations U4 and U26 as shown on the Assembly Diagram.
- () 15. Insert and solder the three 74LS04's at locations U5, U35 and U45 as shown on the Assembly Diagram.
- () 16. Insert and solder the four 8212's at locations U8 through U11 as shown on the Assembly Diagram.
- () 17. Insert and solder the five 74LS161's (or 74LS163's) at locations U12 through U14, U27 and U47 as shown on the Assembly Diagram.
- () 18. Insert and solder the one 75189 at location U15 as shown on the Assembly Diagram.
- () 19. Insert and solder the one 75188 at location U16 as shown on the Assembly Diagram.
- () 20. Insert and solder the one 74LS05 at location U17 as shown on the Assembly Diagram.
- () 21. Insert and solder the one 74LS30 at location U18 as shown on the Assembly Diagram.
- () 22. Insert and solder the three 74LS86's at locations U21, U37 and U40 as shown on the Assembly Diagram.
- () 23. Insert and solder the one 7432 at location U22 as shown on the Assembly Diagram.
- () 24. Insert and solder the four 74367's at locations U6 and U41 through U43 as shown on the Assembly Diagram.

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Assembly Instructions

- () 25. Insert and solder the one 74LS155 in location U23 as shown on the Assembly Diagram.
- () 26. Insert and solder the two 74LS395's at locations U24 and U25 as shown on the Assembly Diagram.
- () 27. Insert and solder the two 74LS00's at locations U29 and U46 as shown on the Assembly Diagram.
- () 28. Insert and solder the one 74LS32 at location U30 as shown on the Assembly Diagram.
- () 29. Insert and solder the one 74LS153 at location U31 as shown on the Assembly Diagram.
- () 30. Insert and solder the two 74LS293's at locations U32 and U33 as shown on the Assembly Diagram.
- () 31. Insert and solder the one 8T20 at location U34 as shown on the Assembly Diagram.
- () 32. Insert and solder the one 74LS74 at location U36 as shown on the Assembly Diagram.
- () 33. Insert and solder the one 74LS51 at location U38 as shown on the Assembly Diagram.
- () 34. Insert and solder the two 74123's at locations U39 and U48 as shown on the Assembly Diagram.
- () 35. Insert and solder the 40 pin solder tail socket at location U7 as shown on the Assembly Diagram.

DISCRETE COMPONENT INSTALLATION

- (✓) 36. Insert and solder the seventeen .1uF disk capacitors at locations C2 through C5 and C8 through C20 as shown on the Assembly Diagram.
- (✓) 37. Insert and solder the ²²33uF tantalum capacitor at location C1 as shown on the Assembly Diagram.
NOTE: Observe polarity (+ to +) as shown on the board.
- (✓) 38. Insert and solder the two ^{.1}.02uF capacitors at locations C6 and C7 as shown on the Assembly Diagram.
- (✓) 39. Insert and solder the ⁴⁴⁵⁴1N914 diode at location CR3 as shown on the Assembly Diagram.

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Assembly Instructions

- () 40. Insert and solder the 1N4742 zener diode at location CR1 as shown on the Assembly Diagram.
- () 41. Insert and solder the 1N751 zener diode at location CR2 as shown on the Assembly Diagram.
- (✓) 42. Insert and solder the 2N3906 transistor at location Q1 as shown on the Assembly Diagram.
- () 43. Insert and solder the four 16 pin sockets at locations U1, U2, U19 and U44 as shown on the Assembly Diagram. SW SW

REGULATOR AND HEAT SINK INSTALLATION

- () 44. Before installing the heat sink and regulator, bend the 7805 regulator leads at 90 degree angles to facilitate mounting on the heat sink.
- () 45. Insert a #6 screw through the 7805 regulator and heat sink on the component side of the board and attach through the lockwasher and nut on the circuit side of the board. Tighten the screw carefully to insure proper alignment of the heat sink to prevent shorting to adjacent traces. Solder in the 7805 regulator leads.
- () 46. Insert and solder the 78L12 regulator at location U49 as shown on the Assembly Diagram, above and to the left of the heat sink.
- () 47. Insert and solder the lead sockets in the jumper pads in the various jumper areas. In most of these areas, the jumper pads are in lines, spaced on 0.1 inch centers, the same spacing as the lead sockets on their carriers. This allows you to insert the sockets in groups and hold them with the carrier while you solder them.
- () 48. Insert and solder the eight cambion pins. Four should be soldered at the location labeled CRI INPUT, and four at the location labeled CRI OUTPUT. These sets of holes are located up between U4 and U5, and up to the left of U8 respectively.

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Assembly Instructions

- () 49. Finally, the UART chip, TR1602 or alternate, should be inserted in its socket at U7 with Pin 1 down toward the 100 pin edge connector at the bottom of the board. Addressing and baud rate jumpers should be installed and other option jumpers installed as required (see the User Guide). The board is ready for use.

MIO USER GUIDE

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- II Address Selection
 - Table 1 - Group Address Selection
 - Table 2 - Internal Address Selection
- III Control Port
 - Table 3 - CRI and PIO Control
 - Table 4 - PIO and SIO Status Selection
 - III.1 Input Jumper Area
 - Table 5 - IJA Signal Definition
 - III.2 Output Jumper Area
 - Table 6 - OJA Signal Definition
- IV SIO Port Procedures
 - IV.1 Hardware Jumpers
 - Table 7 - UART Configuration
 - Table 8 - Baud Rate Jumper Area
 - IV.2 External Interface Connections
 - Figure 1 - Direction Configuration for EIA Connections
 - Table 9 - SIO Connector Signal Definition
 - IV.3 SIO Test Programs
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 - Table 11 - Standard Bit Rates
 - Phase Jumpers

VI (continued)

- VI.2 External Interface Connections
- VI.3 Initial Adjustments
- VI.4 CRI Recording and Reading Procedures
- VI.5 CRI Test Programs

VII Peripheral Interfacing

- VII.1 RS-232-C EIA Interfacing
 - Table 12 - RS-232-C Signals
- VII.2 Serial Current Loop Interface
 - Table 13 - ASR33 and KSR33 Connections
- VII.3 Parallel Interface
- VII.4 Jumper Example Illustrations
 - Figure 2 - Jumper Area Map
 - Figure 3 - Teletype (TM) Jumpers
 - Figure 4 - ADM-3 Jumpers
 - Figure 5 - Tarbell Cassette Jumpers
 - Figure 6 - Byte/Lancaster Cassette Jumpers
 - Figure 7 - AP-44 Printer Jumpers
 - Figure 8 - Key-1 Keyboard Jumpers

APPENDICES - Test and Debugging Information

- Appendix A - Test Cassette Description
- Appendix B - Test and I/O Handling Software
- Appendix C - CRI Initialization Software
- Appendix D - Debugging Information
 - Table 14 - Test Program Addressing and Control
 - Figure 9 - Jumper Settings for Test Programs
 - Figure 10 - Cable M Assembly Drawing
- Appendix E - Component Illustrations

IGENERAL

The MIO board gives the User the following capabilities:

- one serial I/O port
- two parallel I/O ports
- one cassette I/O port
- one control port

NOTES ON THE USER GUIDE

The information which is needed to set-up and use the MIO board is divided into two classes: 1) information which is common to all types of I/O ports used on the MIO board; and 2) information which is required to set up a particular type of port. The USER GUIDE is structured to parallel this division.

Two sections of the USER GUIDE (II. Address Selection and III. Control Port Operation) contain information pertaining to the operation of all I/O ports (CRI, SIO, PIO-1, and PIO-2) used on the MIO board. The User is advised to read these sections before going on to the individual procedures for the SIO, PIO, or CRI ports.

The sections devoted to the individual ports (SIO Procedures, PIO Procedures, and CRI Procedures) include all information for setting up, using, and testing that particular type of port. This includes information on interface connections, jumper options, software access, and test program procedures and listings.

All test programs (Appendix B & C) assume the jumper settings shown in figure 9. If a jumper or jumper area is not mentioned, no particular configuration is required.

ORDER OF INSTALLATION

To avoid having to continually enter the test programs from the front panel, it is advisable to complete the CRI interface before going on to the SIO or PIO ports. The test cassette can then be used to load Test Programs for checking the other ports (see Appendix A for a description of the test cassette).

II.....ADDRESS SELECTION

Address selection for the MIO board consists of: 1) SELECTING A GROUP of 4 I/O port addresses; and 2) CONFIGURING the 4 I/O ports within the selected group of 4 I/O port addresses.

Address selection is achieved through the use of THE EXTERNAL ADDRESS JUMPER AREA and THE INTERNAL ADDRESS JUMPER AREA.

EXTERNAL ADDRESS JUMPER AREA = PCB "BD.ADDJMP."

The External Address Jumper Area selects one group of four I/O port addresses out of the 64 possible groups of addresses that the MIO board may occupy. This is accomplished by selecting Address bits 2-7 at jumper position U19.

Table 1 shows the relationship between a jumper position and an address bit. NOTE that jumper numbers 7 and 8 are USED FOR THE CRI CHANNEL.

For any given address bit, a ONE is selected if a jumper is installed in the corresponding jumper position. A ZERO is selected if no jumper is installed.

Table 1. Group Address Selection

<u>Jumper</u>	<u>IC Pins</u>	<u>Address Bits</u>
1	8, 9	7
2	7, 10	6
3	6, 11	5
4	5, 12	4
5	4, 13	3
6	3, 14	2
7	2, 15	CRI
8	1, 16	CRI

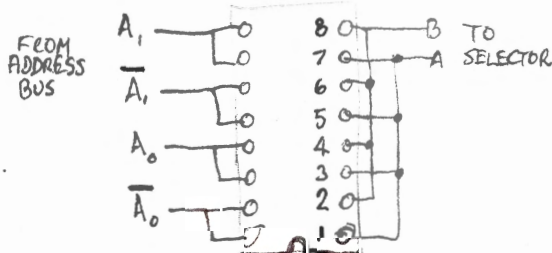
INTERNAL ADDRESS JUMPER AREA

Table 2 shows the possible combinations. All legal jumper combinations are shown. The comment column indicates the hardware (and software) compatibility of the port combinations assuming the appropriate status inputs for the given application have been selected in the Input Jumper Area (see Section III.1).

TABLE 2 - Internal Address Selection

Jumpers Inserted ADDRESS BITS A_0 & A_1

(Pin Number)	Port Numbers	Port Referenced	Comments
	0	CRI <i>cassette</i>	
1 (8, 9)	1	PIO <i>parallel</i>	IMSAI SIO
	2	SIO <i>serial</i>	
6 (3, 14)	3	CONT <i>rol</i>	
	0	PIO	
1 (8, 9)	1	CRI	Processor Tech 3P+S
	2	CONT	
8 (1, 16)	3	SIO	
	0	SIO	
3 (6, 11)	1	CONT	
	2	CRI	
6 (3, 14)	3	PIO	
	0	CONT	
3 (6, 11)	1	SIO	Altair SIO
	2	PIO	
8 (1, 16)	3	CRI	
	0	CRI	Use Parallel port to be compatible with IMSAI SIO Software
2 (7, 10)	1	SIO	
	2	PIO	
5 (4, 13)	3	CONT	
	0	PIO	
4 (5, 12)	1	CONT	
	2	CRI	
5 (4, 13)	3	SIO	
	0	SIO	
2 (7, 10)	1	CRI	
	2	CONT	
7 (2, 15)	3	PIO	
	0	CONT	Use Parallel port to be compatible with Altair SIO Software
4 (5, 12)	1	PIO	
	2	SIO	
7 (2, 15)	3	CRI	



III.....THE CONTROL PORT

The CONTROL PORT is a complete 8 bit Input/Output Port used for internal and external control functions. The operation of the Control Port is easily understood if we separate its functions into two categories: 1) Input Functions; and 2) Output Functions.

CONTROL PORT INPUT FUNCTIONS

As an input port, the eight bits of the Control Port serve to monitor 1) the status of the CRI, SIO, and PIO ports; and 2) external I/O control lines. All input functions of the Control Port are determined by the configuration of the INPUT JUMPER AREA (IJA).

CONTROL PORT OUTPUT FUNCTIONS

As an output port, the eight bits of the Control Port are used for external and internal control functions according to the following division.

1. BITS 0-3

Bits 0-3 are latched and used to control external devices when needed. The function of these bits are determined by the configuration of the OUTPUT JUMPER AREA (OJA).

2. BITS 4-7

Bits 4-7 are latched and serve three functions: 1) to control CRI functions;
2) to select PIO ports 1 or 2; and
3) to decode the status signals PIOS and SIOS.

TABLE 3 shows the decoding of bits 4-7.

If either of the two status signals PIOS or SIOS are used as an input to the Control Port, bits 6 and 7 of the Control Port output word are used to determine which of the error

lines are active. The decoding for this function is shown in Table 4.

Table 3 - Control of CRI and PIO

CONT BIT	VALUE	USE
4	1	Enable CRI Write Circuitry
	0	Disable CRI Write Circuitry
5	1	Enable CRI Read Circuitry
	0	Disable CRI Read Circuitry
6	1	Enable CRI Ready on each bit
	0	Enable CRI Ready on each byte
7	1	Select PIO Port 2
	0	Select PIO Port 1

Table 4 - Control Selection of PIO and SIO Status

Value of Control Signal Available from Input Selector

Bit 7	Bit 6	PIOS	SIOS
0	0	Port 1 Output Data Ready	Error = PE or FE or OE
0	1	Port 1 Input Data accepted	Overrun Error (OE)
1	0	Port 2 Output Data Ready	Parity Error (PE)
1	1	Port 2 Input Data accepted	Framing Error (FE)

III.1INPUT JUMPER AREA

"JUMPER AREA MAP"

The "INPUT JUMPERS" AREA is organized as shown in figure 2. Row A contains the 8 input bits of the Control Port. Rows B, C, and D contain three types of signals: 1) the status input sources; 2) the serial data input to the UART; and 3) the output of EIA, TTL, and Current Loop receivers used for receiving serial data and I/O control lines. Row E contains 8 Ground connection points and Row F contains the 8 vectored interrupt lines. All signals are defined in TABLE 5 by location and signal name.

FUNCTIONS

The INPUT JUMPER AREA serves four functions.

- 1) It allows the User to jumper any of the status input sources located in Rows B, C, and D to any of the 8 input bits of the Control Port (Row A).
- 2) It allows the User to jumper EIA and TTL receivers connected to I/O control lines (Rows C and D) to any of the 8 input bits of the Control Port (Row A).
- 3) It allows the User to jumper the Serial Data Line to Current Loop Receivers, EIA Receivers, or TTL Receivers for the SIO Channel of the MIO Board.
- 4) It allows the User to jumper any of the Vectored Interrupt Lines contained in Row F to any of the status input sources contained in Rows B, C and D.

Table 5: Input Jumper Area Signal Definition

<u>Location</u>	<u>Signal Name</u>	<u>Description</u>
A0 thru A7	SIO thru SI7	Data Input for Bits 0-7
B0	OE	SIO UART Overrun Error
B1	SIOS	Determined by CNTL, see Table 4
B2	/RRDY	Logical Inversion of RRDY
B3	/TRDY	Logical Inversion of TRDY
B4	TRDY	SIO UART Ready for Transmit Data
B5	FE	SIO UART Framing Error
B6	RRDY	SIO UART has Received Data Ready
B7	PE	SIO UART Parity Error
C0	RDATA	SIO UART Receive Data Input Line
C1	CL1	Current Loop Input Data (+ on J4-8, - on J4-22)
C2	PRDY	O1DA or I1DR or O2DA or O2DR
C3	PIOS	Determined by CNTL, see Table 4
C4	I2DA	PIO Port 2 is Ready for More Output Data
C5	O2DR	PIO Port 2 has Input Data Ready
C6	I1DA	PIO Port 1 is Ready for More Output Data
C7	O1DR	PIO Port 1 has Input Data Ready
D0	REIA4	EIA Receiver Number 4
D1	REIA3	EIA Receiver Number 3
D2	REIA2	EIA Receiver Number 2
D3	REIA 1	EIA Receiver Number 1
D4	CRIS	Bit Ready or Byte Ready from CRI
D5	ITTL3	TTL Direct Input 3 (J9-12)
D6	ITTL2	TTL Direct Input 2 (J4-6)
D7	ITTL1	TTL Direct Input 1 (J4-16)
E0 thru E7	Ground	For Disabling Interrupts or Zeroing Data Bits
F0 thru F7	V10 thru V17	Interrupt Request Selects

SOURCE DEFINITIONS

The possible sources in ROWS B, C, and D are defined as follows.

B0-B6

B0-B6 are status signals used for the SIO channel. Note that B1, (SIOS) is a logical OR'ing of PE, FE, and OE. If this signal is used, the Control Port output word allows the User to decode this signal to determine which error (PE, FE, or OE) occurred. This is covered in CONTROL PORT OUTPUT FUNCTIONS.

FROM V30 #031
IF SELECTED THROUGH 031

C0-C6

C0 is the Serial Data which is to be input to the SIO Channel.

C1 (CL1) is the Current Loop Receiver for the SIO Channel.

C2-C7 are status signals used for the two PIO channels. Note that C2 and C3 are the logical OR'ing of the signals I1DA, O1DR, I2DA, and O2DR. If C3 (PIOS) is used, the Control Port output word allows the User to decode this signal to determine which of the four error lines is active. This is covered in the section, CONTROL PORT OUTPUT FUNCTIONS.

D0-D7

D0-D3 provide for 4 EIA Receivers to be used with the SIO Channel.

D4 is a status line used for the Cassette Channel to indicate when a bit or byte is ready.

D5-D7 provide for three TTL level inputs for the SIO Channel.

E0-E7

E0-E7 provide for 8 Ground points.

F0-F7

F0-F7 provide for the 8 Vectored Interrupt Lines.

NOTE

The configuration needed for each type of port will be covered in the SIO, CRI, and PIO Procedures.

III.2.....OUTPUT JUMPER AREA

The OUTPUT JUMPER AREA is located at position U2 on the MIO Board, and is organized into three groups.

- 1) Pins 13-16 are the output bits 0-3 of the Control Port.
- 2) Pin 12 is the Serial Transmit Data from the SIO Channel.
- 3) Pins 1-8,10,11 are Drivers for EIA, TTL,CURRENT LOOP, and HIGH VOLTAGE (40v. 40Ma) levels.
- 4) 9 is Ground

The signals present at the Output Jumper Area are defined in Table 6.

FUNCTIONS

The OUTPUT JUMPER AREA serves two functions.

1. It allows the User to jumper the Serial Transmit Data from the SIO Channel to any one of the three types of output drivers (EIA, TTL, and Current Loop).
2. It allows the User to jumper Control output bits 0-3 to any of the output drivers to be used as I/O Control Lines.

The configuration needed for each type of port will be covered in the SIO, PIO, and CRI Procedures.

NOTE

If the Current Loop Driver is not used, it should be jumpered to the Ground signal at pin 9 of the OUTPUT JUMPER AREA.

Table 6 Output Jumper Area Signal Definitions

<u>PIN#</u>	<u>SIGNAL NAME</u>	<u>DESCRIPTION</u>
16	CR0	Control Register Bit 0
15	CR1	Control Register Bit 1
14	CR2	Control Register Bit 2
13	CR3	Control Register Bit 3
12	TDATA	SIO UART Serial Transmit Data
11	OTTL1	TTL Direct Output 1 (J4-10)
10	OTTL2	TTL Direct Output 1 (J4-2)
9	GND	Ground
8	DEIA1	EIA Transmitter Number 1
7	DEIA2	EIA Transmitter Number 2
6	DEIA3	EIA Transmitter Number 3
5	DEIA4	EIA Transmitter Number 4
4	OC1	High Voltage (40V) Power (40MA) Driver 1 (J4-23)
3	OC2	High Voltage (40V) Power (40MA) Driver 2 (J4-4)
2	OC3	High Voltage (40V) Power (40MA) Driver 3 (J4-19)
1	CLO	Current Loop Output (+on J4-20, -on J4-24)

IV.....SIO PORT PROCEDURES

The SIO Port is a full 8 bit serial input/output port. It is used in conjunction with the Control Port, which in this case allows the User to 1) read selected status lines from the UART: and 2) read and write on external I/O control lines.

Setting up the SIO Port involves three steps:

1. configuring the hardware jumpers;
2. making the external interface connections; and
3. running test programs to check out the operation of the port.

IV.1...HARDWARE JUMPERS

INPUT JUMPER AREA

In the INPUT JUMPER AREA:

1. The serial data from the appropriate receiver (TTL, EIA, or Current Loop) must be jumpered to the RDATA terminal (C0) to be input to the UART.
2. The desired UART status signals and external control signals must be jumpered to the Control Port inputs. The UART status signals are available at Row B (B0-B7) and need to be jumpered to the desired input bit of the Control Port, available at Row A (A0-A7). Any external control signals will be taken from the appropriate type of receiver (TTL or EIA) and jumpered to the desired bit of the Control Port (Row A).

OUTPUT JUMPER AREA

In the OUTPUT JUMPER AREA:

1. The serial data from the UART (U2-12) must be jumpered to the appropriate transmitter (EIA, TTL, or Current Loop).
2. The output bits 0-3 of the Control Port must be jumpered to the appropriate type of transmitter (EIA, TTL, or OC) to be used as external control signals.

SIO STATUS SIGNALS

PE - If a Parity Error occurs, PE goes high;
FE - If a Framing Error occurs, FE goes high;
OE - If an Overrun Error occurs, OE goes high;
SIOS - If any of the signals, PE, FE, or OE, are active, SIOS will go high. The type of error which occurred may be determined by using the Control Output Port bits 6 and 7 as shown in Table 4.
TRDY, TRDY - UART Transmitter Ready; and
RRDY, RRDY - UART Receiver Ready.

These signals are most typically used by jumpering them in the Output Jumper Area to bits of the Control Port (column A of the OJA).

SIO CONFIGURATION JUMPER AREA

The UART can be configured to transmit and receive a variety of character lengths and parity configurations. The SIO Configuration Jumper Area is used to hardwire the configuration desired. It provides +V (for a logic 1) on Row B and Ground (for a logic 0) on Row A for connection to the configuration inputs in Row C. Table 7 defines these inputs. Note that all inputs connected to +V provide the standard TTY configuration.

Table 7. UART Configuration Definition

SIGNAL	VALUE	UART OPERATION
PI	1	Do not transmit or check parity
	0	Transmit and check parity
SBS	1	Transmit 1.5 stop bits for 5 bit characters, 2 for all others
	0	Transmit 1 stop bit per character
WLS1 &	00	5 Bits/Character
WLS2	01	6 Bits/Character
	10	7 Bits/Character
	11	8 Bits/Character
EPE	1	Generate and check Even Parity
	0	Generate and check Odd Parity

SIO BAUD RATE SELECTION

The Baud rate for the UART is formed by dividing down Phase II. This permits the User to select virtually any rate between 45.5 and 9600 baud. The division is accomplished by presetting a 12 bit counter and incrementing it to a value of 4084, at which time it is reloaded. The formula for determining the preset value is: (in base 10)

= $\frac{S_{100}}{\text{CLOCK}}$

$$P.V. = 4085 - (125,000/\text{BAUD RATE})$$

In the SIO BAUD RATE JUMPER AREA, Row A provides Ground (used when the preset is a 0), Row B provides +V (used when the preset is a 1), and Row C is the counter input. Table 8 gives the preset value for standard BAUD rates.

Table 8 - Baud Rate Jumper Selections

BAUD RATE	PRESENT VALUE	HEX REP.	BINARY VALUE BY BIT (MSB=11)											
			11	10	9	8	7	6	5	4	3	2	1	0
9600	4072	FE8	1	1	1	1	1	1	1	0	1	0	0	0
4800	4059	FDB	1	1	1	1	1	1	0	1	1	0	1	1
2400	4033	FC1	1	1	1	1	1	1	0	0	0	0	0	1
1200	3981	F8D	1	1	1	1	1	0	0	0	1	1	0	1
600	3877	F25	1	1	1	1	0	0	1	0	0	1	0	1
300	3668	E54	1	1	1	0	0	1	0	1	0	1	0	0
150	3252	CB4	1	1	0	0	1	0	1	1	0	1	0	0
134.5	3156	C54	1	1	0	0	0	1	0	1	0	1	0	0
110	2949	B85	1	0	1	1	1	0	0	0	0	1	0	1
75	2418	972	1	0	0	1	0	1	1	1	0	0	1	0
45.5	1338	53A	0	1	0	1	0	0	1	1	1	0	1	0

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IV.2EXTERNAL INTERFACE CONNECTIONS

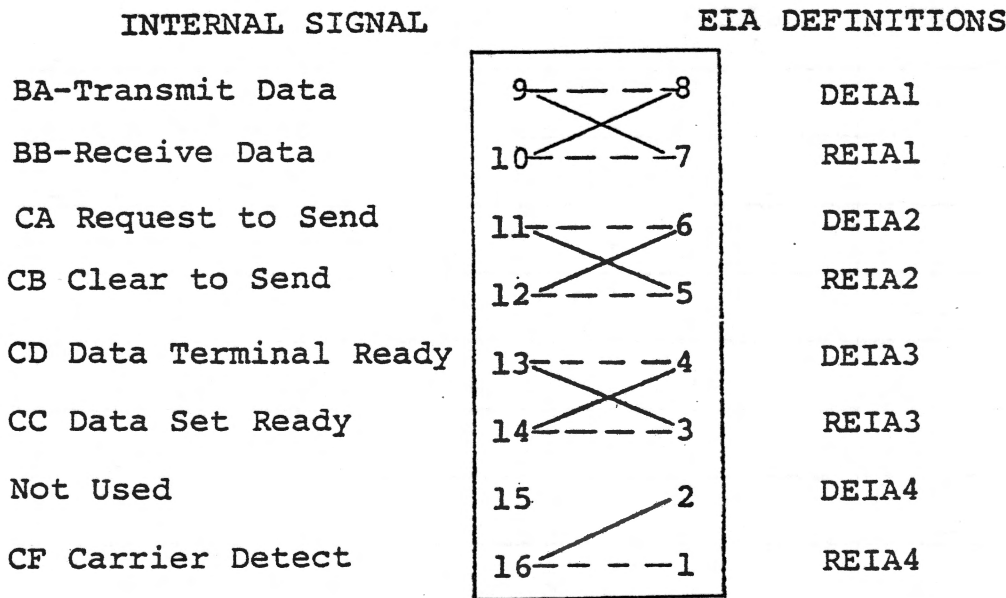
EIA CONNECTIONS

Table 9 gives the signal names for the SIO connections to the 26 pin edge connector and the corresponding EIA 25 pin connector number. Signals marked with an asterisk are standard RS232 definitions. The RS232 definition is given with respect to the terminal.

DIRECTION JUMPER AREA

The DIRECTION JUMPER AREA allows the SIO port to act as the computer or terminal end of an EIA RS232 line. Figure 1 shows the configuration for the two modes of operation.

Figure 1: Direction Configuration for EIA



————— Connections Made to run complete EIA interface with a terminal
 ----- Connections made to run complete EIA interface with a modem

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Table 9
SIO CONNECTOR (J4) SIGNAL DEFINITION

<u>MIO Edge Connector</u>	<u>EIA Connector</u>	<u>Signal Name</u>
1	1	Chassis Ground AA*
2	14	TTL Out 2
3	2	Transmit Data BA*
4	15	Open Collector Out 3
5	3	Receive Data BB*
6	16	TTL in 1
7	4	Request to Send CA*
8	17	Current Loop in +
9	5	Clear to Send CB*
10	18	TTL Out 1
11	6	Data Set Ready CC*
12	19	TTL in 2
13	7	Signal Ground AB*
14	20	Data Terminal Ready CD*
15	8	Carrier Detect CF*
16	21	TTL in 3
17	9	+5 Volts
18	22	-----
19	10	Open Collector Out 2
20	23	Current Loop Out +
21	11	EIA Driver or Receiver
22	24	Current Loop In -
23	12	Open Collector Out 1
24	25	Current Loop Out -
25	13	-----
26	--	-----

* EIA Standard Signal
Designation

CURRENT LOOP CONNECTIONS

The Current Loop Signals are:

- 1) IN+ (J4-8)
- 2) IN- (J4-22)
- 3) OUT+ (J4-20)
- 4) OUT- (J4-24).

Resistors R9 and R12 are defined to be 1.2K Ohms on the schematic. These resistors provide for 20 mA Current Loops on both Input and Output. If a 60 mA Current Loop is needed, the values of these two resistors should be changed to 100 Ohms.

IV.3.....SIO TEST PROGRAMS

There are four test programs which can be used with the SIO. To use the test programs the board should have the status bits configured as defined in Section 1.

SIO TEST 1

The board should be jumpered to interface with the peripheral to be used for this test. The starting address is 3100H. The value of the sense switches is continuously output as a character; and an input character (if any) is displayed in the Sense Lights. The Sense Lights will display the last character until a new character is received. If an error occurs, the Sense Lights will be set to all ones. The program will pause for fifteen seconds each time the value of the Sense Switches is changed.

SIO TEST 2

The board should be jumpered to interface with the peripheral to be used for this test. The starting address is 3103H. The SIO RRDY signal is continuously monitored and each time a character is received, it is transmitted to the SIO output. Errors on input cause the character to be ignored.

SIO TEST 3

The board should be jumpered to connect the SIO serial output to the SIO serial input for this test. The starting address is 3106 H.

The Sense Switches are used to define any bits which should not be transmitted as part of this test. Switches should be set to a zero for all bit positions to be transmitted (i.e., for seven bits, the MSB is set; for 6 bit, the two MSBs are set; etc.). If you leave your terminal connected to the board while running this test, do not attempt to type in as this will generate an error.

The test continuously transmits all possible binary combinations within the pattern and compares the received results. If the test is running without error, the Sense Lights will all be out.

If a PE, OE, or FE occurs, the program will display 0FF Hex until one of the Sense Switches is changed. When a change is made, these errors are displayed in positions 4, 3, and 2 respectively. Changing the Sense Switches will cause the program to continue. If a failure occurs in the transmitted value versus received value, the program will display 0FE Hex. Changing of the Sense Switches will cause the value of the transmitted character to be displayed in the Sense Lights.

Changing the Sense Switches a second time will cause the value of the received character to be displayed in the front panel lights. Changing of the Sense Switches will also cause the program to continue with the next value.

V PIO PORT PROCEDURES

The two parallel I/O ports available on the MIO are both addressed with the same I/O address from the 8080. The ports are multiplexed using bit 7 of the Control Output word as discussed in Section III. The two ports operate identically and have identical external interfaces on J2 and J3.

The two PIO Ports are used in conjunction with the Control Port, which in this case allows the User to read selected Status Signals from either or both ports.

The PIO Output Ports each contain eight output data lines and three control lines. The PIO Input Ports each contain 8 input data lines and two control lines.

Setting up the PIO Port involves:

1. configuring the hardware jumpers;
2. making the external interface connections; and
3. running test programs to check out the operation of the port.

V.1 HARDWARE JUMPERS

INPUT JUMPER AREA

In the INPUT JUMPER AREA:

The PIO status signals (C3 - C7) must be jumpered to the desired input bits of the Control Port (Row A).

PIO STATUS SIGNALS

IDA - Input Data Accepted (as defined in PIO External Interface Connections)

ODR - Output Data Ready (as defined in PIO external Interface Connections)

PIO STATUS SIGNALS (cont.)

PIOS - If any of the signals IDA or ODR goes high, PIOS will go high. The signal which occurred may be determined by using the Control Output Port bits 6 and 7 as shown in Table 4.

INPUT STROBE JUMPER AREA

The INPUT STROBE JUMPER AREA allows the User to select one of five types of input strobe signals. Note that J1 and J3 for PIO port 1 correspond to J2 and J4 for PIO port 2.

If no jumper is placed at J3 (J4 for PIO port 2), the data lines will be monitored but not latched. A jumper is placed from A to C on J3 (J4) if an external pulse is used as the input strobe. A jumper is placed from B to C if edge triggering is to be used.

If J1 (J2 for PIO 2) is present, a positive strobe is selected. If J1 (J2) is omitted, a negative strobe is selected.

V.2 EXTERNAL INTERFACE CONNECTIONS

Table 10 lists the signals to be used in interfacing the two parallel I/O ports with external devices.

PIO CONTROL SIGNALS

The PIO Output Ports each have 3 Control Lines. These are defined as follows:

ODR - an Output Data Ready Line for each port, to indicate to the processor when the output device and thus the output port is ready to receive data. ODR may be monitored using Interrupts or the Control Input Port. This signal can be used as a positive data strobe for the external output device.

PIO CONTROL SIGNALS (cont.)

CODR - a Clear Output Data Ready Line for each port to set the ODR Lines active low. This signal is generated from the external device when it is ready to receive data.

OSTB - a negative Strobe Line is provided from each parallel output port. It may be used as an external strobe to an output device. It has the same timing as PWR.

Normally when an external I/O device is ready to accept data, it asserts CODR, which in turn sets the ODR Line active low. When the processor finishes outputting data to the output port, ODR is reset high, providing a positive strobe to the external output device.

The PIO Input Ports each have two Control Lines. These are defined as follows:

IDA - one Input Data Accepted Line for each port, to indicate to the processor when data has been loaded from the external input device. This line is normally set low when the STB is received from the external device.

ISTB - one Input Strobe Line is provided for each port to strobe the data into the input latches and to set the IDA lines low. This signal originates at the external input device. Data is strobed on the leading edge of ISTB if there is no jumper at J1, and on the trailing edge if jumper J1 is present.

Normally the external input device sends a STB with the data. This latches the data and sets IDA low. When the processor senses IDA low (via Interrupts or the Control Port), it reads the data from the latch which in turn resets IDA high.

Table 10
PIO CONNECTOR (J2 and J3) SIGNAL DEFINITION

<u>MIO EDGE CONNECTOR</u>	<u>EIA CONNECTOR</u>	<u>SIGNAL NAME</u>
1	1	Ground
2	14	+16 Volts
3	2	Output Data Bit 0
4	15	Input Data Bit 0
5	3	Output Data Bit 1
6	16	Input Data Bit 1
7	4	Output Data Bit 2
8	17	Input Data Bit 2
9	5	Output Data Bit 3
10	18	Input Data Bit 3
11	6	Output Data Bit 4
12	19	Input Data Bit 4
13	7	Output Data Bit 5
14	20	Input Data Bit 5
15	8	Output Data Bit 6
16	21	Input Data Bit 6
17	9	Output Data Bit 7
18	22	Input Data Bit 7
19	10	Output Data Ready
20	23	Input Data Accepted
21	11	External Output Strobe
22	24	Input Strobe
23	12	+5 Volts
24	25	-16 Volts
25	13	Output Strobe
26	--	-----

V.3....PIO TEST PROGRAMS

There are three tests shown in Appendix B for the PIO. Test 1 (starting at address 3109 H) continuously reads the Sense Switches and outputs this value to both PIO Ports and to the Sense Lights. Test 2 continuously inputs from PIO Port 1 and outputs to PIO Port 1, PIO Port 2 and the Sense Lights. Test 3, starting at 310F Hex, has the same output as Test 2; the difference is that the input is from PIO Port 2.

To test the inputs using these tests, a jumper wire or test clip can be used to alternately apply ground and +5 volts to each input pin, while observing the effect on the Sense Lights. Ground applied to a pin will turn off the corresponding light, while +5 volts will turn it on. For protection, insert a 470 Ohm resistor in series with the test lead.

To test the outputs, monitor each output pin for the appropriate logic level, as set by the Sense Switches, using a voltmeter, logic probe, or oscilloscope.

VI.....CRI PORT PROCEDURES

The CRI Port supports ANSI (Tarbell) and Byte/Lancaster Formats for storage and retrieval of information to and from cassette tape.

The CRI Port is used in conjunction with the Control Port, which in this case is used to read the status signal, CRIS, indicating whether a bit or byte is ready. The function of CRIS is determined by output bit 6 of the Control Port (Table 3).

ANSI (Tarbell) Formats

Data is recorded on the tape using Biphasic Encoding to directly support the ANSI (Tarbell) data Format. The standard data rate is 1500 bits per second (187 bytes/second). This may be increased depending on the quality of the cassette recorder used.

Byte/Lancaster Formats

1200/2400 Hz bursts = 300 BPS

To support the Byte/Lancaster Format, the software tape handler in Appendix B must be used.

The conversion of Biphase Data Formats into Byte/Lancaster Formats is explained in the following discussion. Biphase Encoding results in two flux reversals per bit (one cycle) when recording a constant string of ones or zeros; and one flux reversal per bit (one-half cycle) when recording a string of alternating ones and zeros (see the Theory of Operation for more detail). Hence, recording a byte of all ones in the Biphase mode results in eight cycles being recorded. Recording a byte of alternating ones and zeros (e.g., 1010 1010 AA Hex) results in four cycles being recorded.

The Byte/Lancaster standard for recording data is then achieved by changing the recording speed to 2400 bits/second and recording a byte of FF Hex or 55 Hex to represent a one or zero bit respectively. For more detailed information, the User is referred to the article by Lancaster in the first issue of Byte Magazine.

DATA FORMATS

Writing a block of data to cassette consists of writing a Start Byte (for synchronizing the hardware data separation logic), a Sync Byte (for software recognition as a start-of-block indicator), the data bytes, and a check byte(s).

Reading the data back requires recognizing the Sync Byte, reading and storing the data bytes and then using the check bytes to insure the data was properly transferred.

Appendix B contains subroutines for writing the Start and Sync Bytes, writing a Data Byte, recognizing the Sync Byte and reading a Data Byte. Also included are handlers for writing or reading a block of 256 bytes using the standard CRC data check for insuring that the data is proper.

The routines listed in Appendices B and C are recorded in Tarbell format on the test cassette which is shipped with the board. The cassette is more fully described in Appendix A.

Setting up the CRI Port involves:

1. configuring the hardware jumpers;
2. making the external interface connections; and
3. running test programs to check out the operation of the port.

VI.1 ... HARDWARE JUMPERS

INPUT JUMPER AREA

In the INPUT JUMPER AREA:

The status signal CRIS (D4) must be jumpered to the desired input bit of the Control Port (Row A).

CRIS

This signal goes high to indicate to the processor when a bit or byte is ready. It may be jumpered to the Interrupt Lines or to the Input bits of the Control Port. Note that bit 6 of the Control Output Port is used to select a bit or byte ready (see Table 3).

CRI BIT RATE JUMPER AREA

The bit rate for recording data is formed by dividing down $\emptyset 2$. This permits the User to select any data rate from 488 to 62,500 bits per second. The division is accomplished by presetting an 8 bit counter and counting it up to 255, at which time it is reloaded. The output of this counter is further divided by 16 to form the final recording speed. The formula for determining the preset value is: (in base 10)

$$P.V. = 256 - (125,000/\text{BIT RATE})$$

In the CRI Bit Rate Jumper Area, Row A provides Ground (used when the preset is a zero). Row B provides +V (used when the preset value is a one), and Row C is the counter input. Table 11 gives the standard bit rates.

MIO
Errata
2/18/77

It has come to our attention that to read cassettes on an MIO Board that have been written on a Tarbell Board, the preferred Bit Rate is 1689 BPS.

Add the following line to Table 11: Standard Bit Rate (on page 2-31).

Bit Rate	Preset Value	Hex Repr.	Binary Value by Bit (MSB=7)							
			7	6	5	4	3	2	1	0
1689	182	B6	1	0	1	1	0	1	1	0

ECN 77-0014

The test cassette supplied with your MIO Board has been recorded at 800 bits per second instead of 1500 as implied in the chapter.

Add the following line to Table 11: Standard Bit Rate (on page 2 - 31).

Bit Rate	Preset Value	Hex Repr.	Binary Value By Bit (MSB=7)							
			7	6	5	4	3	2	1	0
800	100	64	0	1	1	0	0	1	0	0

See the attached sheet Figure 5a for setting up the MIO Board to run 800 BPS.

Table 11: Standard Bit Rate

BIT RATE	PRESET VALUE	HEX REPR.	BINARY VALUE BY BIT (MSB=7)							
			7	6	5	4	3	2	1	0
4800	230	E6	1	1	1	0	0	1	1	0
2400	204	CC	1	1	0	0	1	1	0	0
1500	173	AD	1	0	1	0	1	1	0	1

RECORDING PHASE JUMPERS

Jumpers 7 and 8 of the External Address Jumper Area serve as the Recording Phase Jumpers. They serve to invert the polarity of the data written to the cassette. This option is determined by the phase of the recorder and the procedures for determining this are given in the CRI Initial Adjustments.

VI.2 ... EXTERNAL INTERFACE CONNECTIONS

Sockets are provided on the MIO Board for two each input and output lines for the CRI interface. This allows interface to two cassette recorders simultaneously, though only one may be read at a time

An optional cable set (IMSAI Cable M) is available to bring the cassette lines out to the back panel to the 8080 chassis. It terminates in a standard miniature phone jack at the back panel. Two cables, one for input and one for output, are included in each set, and one set is required for each recorder to be interfaced.

VI.3 ... Initial Adjustments

The adjustments required for operating consist of finding the proper volume settings for recording and reading back the data, and setting the interface so that it reads and writes in the proper phase (using jumper 7 and 8 respectively in the External Address Jumper Area). First find the input settings as follows:

1. Insert the test cassette to read on side 1.
2. Set the tone control on your recorder for best high frequency response.
3. Turn the volume to a middle position.
4. Load the Sync Recognition Program from Appendix C using the front panel switches.
5. Start the program at location 3000 Hex.
6. Press the "play" button on your recorder.
7. Adjust the volume until the Sense Lights are all 1's. When the Sync Byte is recognized, the Sense Lights will all be 1, otherwise 0. If the lights are all 1's, go to step 9.
8. If the Sense Lights do not come on, insert Jumper 7 in the External Address Jumper Area. This will reverse the playback phase the interface uses. Repeat Step 7.
9. Adjust the volume in both directions until the Sense Lights go out. The middle setting of this range should be used for all future reading data.

Now, the appropriate output setting should be found as follows:

1. Insert a BLANK tape into your recorder.
2. Load the Sync Generation Program from Appendix B using the front panel switches.
3. Adjust your volume control to lowest position.
4. Start the program at location 301F Hex.
5. Start the recorder in record mode.
- *6. Slowly and uniformly increase the volume until it reaches the maximum. This should be done so when the tape is read you can use the timing relationship to determine the best recording volume.

* On some recorders with AGC, the volume control has no effect on recording signals. Omit step 6 in these cases.

7. Rewind the tape and read the tape using the program from above and playback volume determined there. Use the Sense Lights to determine the best recording volume.
8. If the Sense Lights do not come on during step 7, insert Jumper 8 in the External Address Area (to reverse the recording phase) and repeat the above steps.

VI.4 ...CRI Recording and Reading Procedures

You are now ready to use your recorder to read in the programs from Appendix B. The object programs start about 3 minutes and 30 seconds from the start of the tape. The first 3 minutes is a sync stream consisting of recorded E6's; the next 30 seconds is $\emptyset\emptyset$'s and after this are the MIO test programs. The steps to be used whenever recording or reading data are given below.

For recording a data block:

1. Turn the volume control all the way down.
2. Position the tape to the desired recording location.
3. Get to the point in the program where you can start recording with the push of a button.
4. Start the cassette recorder and slowly increase the volume to the proper setting.
5. Wait 5 seconds for writing leader, then start the program.
6. Stop the cassette when the program indicates the write operation is complete.

For Reading a data block:

1. Set the volume control to the playback position determined during the initial adjustment procedure.
2. Position the tape to the desired playback position (2 or 3 seconds into the leader).
3. Get to the point in the program where you can start reading with the push of a button.
4. Start the cassette in the playback mode and then start the program.
5. Stop the cassette when the program indicates the read operation is complete.

To read the object program from Appendix B, load the Bootstrap Program contained in Appendix A. Use the read procedure as defined above with the following additions.

1. Start tape position is 3 minutes and 30 seconds into side 1 of the tape.
2. Starting address for Bootstrap Program is 3800 Hex.
3. Programs will be completely loaded in 20 seconds.
4. The Programmed Output light will go out when finished

VI.5 ... CRI TEST PROGRAMS

To test the operation of your cassette with the CRI, two steps are required. First, use the block recording procedure to write a block of data onto a blank tape. The program to do this is contained in Appendix B and starts at location 3112 Hex. The Sense Lights are initially set to COH, program completion is indicated by the lights going to 0. Then read the block using the read procedure and the program contained in Appendix A with a Starting Address of 3115 Hex. Successful completion of the read is indicated by the sense lights going to zero. Sense light read-out of FFH indicates a CRC error. Changing of the sense switches will cause the data compare to be done. Sense light read-out FEH indicates a data compare error. In this case, changing the switches once causes the display of the byte error (this is also the data). The second change causes the bad data to be displayed and the third time causes the compare to continue.

VII.... PERIPHERAL INTERFACING

This section will define the jumper configurations required to interface the MIO board with different types of peripherals. An example will be given for standard serial EIA interfaces, serial current loop interfaces (for teletypes) and a parallel interface. Prior to reading this section, the reader should review Section 1.2 as a refresher of the standard jumpers assumed. A set of illustrations showing jumper configurations for a number of common peripherals appears at the end of this section. Two worksheets for laying out your own jumpers are included.

VII.1.. RS-232-C EIA Interfaces

In addition to the jumpers specified in Section 1.2, the following two jumpers must be added.

IJA - REIAL to RDATA
 OJA - TDATA to DEIAL
 GND to CLO (to put output current loop in active state)

This provides all of the signals required for the interface to be standard interface. The cable shield or ground should be attached to the pad as indicated on the Assembly Diagram. It should be noted that the SIO Baud Rate and UART Configuration Jumpers must be installed to match the peripheral equipment. Insertion of one of the two possible Direction Configuration Jumpers will then complete the required jumpers. Table 12 shows the signals driven and received in the two configurations.

Table 12 RS-232-C EIA Signals

I/O BITS	TO RUN TERMINAL	TO RUN MODEM
SIO PORT (all)	DATA IN & OUT	DATA IN & OUT
Control IN - BIT 7	REQUEST TO SEND	CLEAR TO SEND
Control IN - BIT 6	DATA TERMINAL READY	DATA SET READY
Control IN - BIT 5	NOT USED	CARRIER DETECT
Control IN - BIT 1	RECEIVED DATA READY	RECEIVE DATA READY
Control IN - BIT 0	TRANSMIT READY	TRANSMIT READY
Control OUT - BIT 2	CARRIER DETECT	NOT USED
Control OUT - BIT 1	CLEAR TO SEND	REQUEST TO SEND

VII.2 .. Serial Current Loop Interface

The simplest current loop interface to a Teletype uses only the serial input and output data lines. Hence, only bits 1 and 0 of the Control Input are used to indicate transmitter and receiver status. Internal to the MIO, the following jumpers must be added.

- IJA - CLI to RDATA
- OJA - TDATA to CLO
- SIO BAUD - Jumper for 110 Baud
- SIO CONFIG - All Jumpers to +V (i.e., Row B to C)

There is a terminal strip located at the right rear of the teletype (ASR33 or KSR33). The terminal strip is behind a panel of square white plastic connectors and also connects to the TTY power cord. The terminals are numbered from 1 to 9. The connections required between the MIO and these terminals are shown in Table 13. In addition to making these connections, it may be necessary to perform the following operations on your teletype.

1. Full Duplex Operation - Move YEL/BRN wire from Terminal 3 to Terminal 5 and move WHT/BLU wire from Terminal 4 to Terminal 5.
2. Change receiver current level from 60 ma to 20 ma; move VIO wire from Terminal 8 to Terminal 9.
3. Change current source resistor to 1450 Ohms. Locate the current source resistor in front of the power supply and move the BLU wire to the tap labelled 1450.

Table 13 Connections for ASR33 and KSR33

Signal Name	26 Pin Edge Connector	25 Pin EIA Connector	Terminal Strip
Current Loop Out +	20	23	7
Current Loop Out -	24	25	6
Current Loop In +	8	17	3
Current Loop In -	22	24	4

VII.3 .. Parallel Interface

The IMSAI Key-1 Keyboard provides an example of a parallel interface. The keyboard uses one PIO input port with its associated handshake signals. The example shown in the illustration at the end of this section uses the processor interrupt request line to signal that an input character is ready, and the interrupt acknowledge to signal acceptance of the character.

Interface Examples

Figure 2 below shows the location of the jumper areas described in the User Guide. Specific examples of the use of these jumpers for interfacing common peripherals are shown on the following pages, followed by a worksheet that you can use to lay-out your own jumper connections.

~~FILE~~ DONE
4-29-83

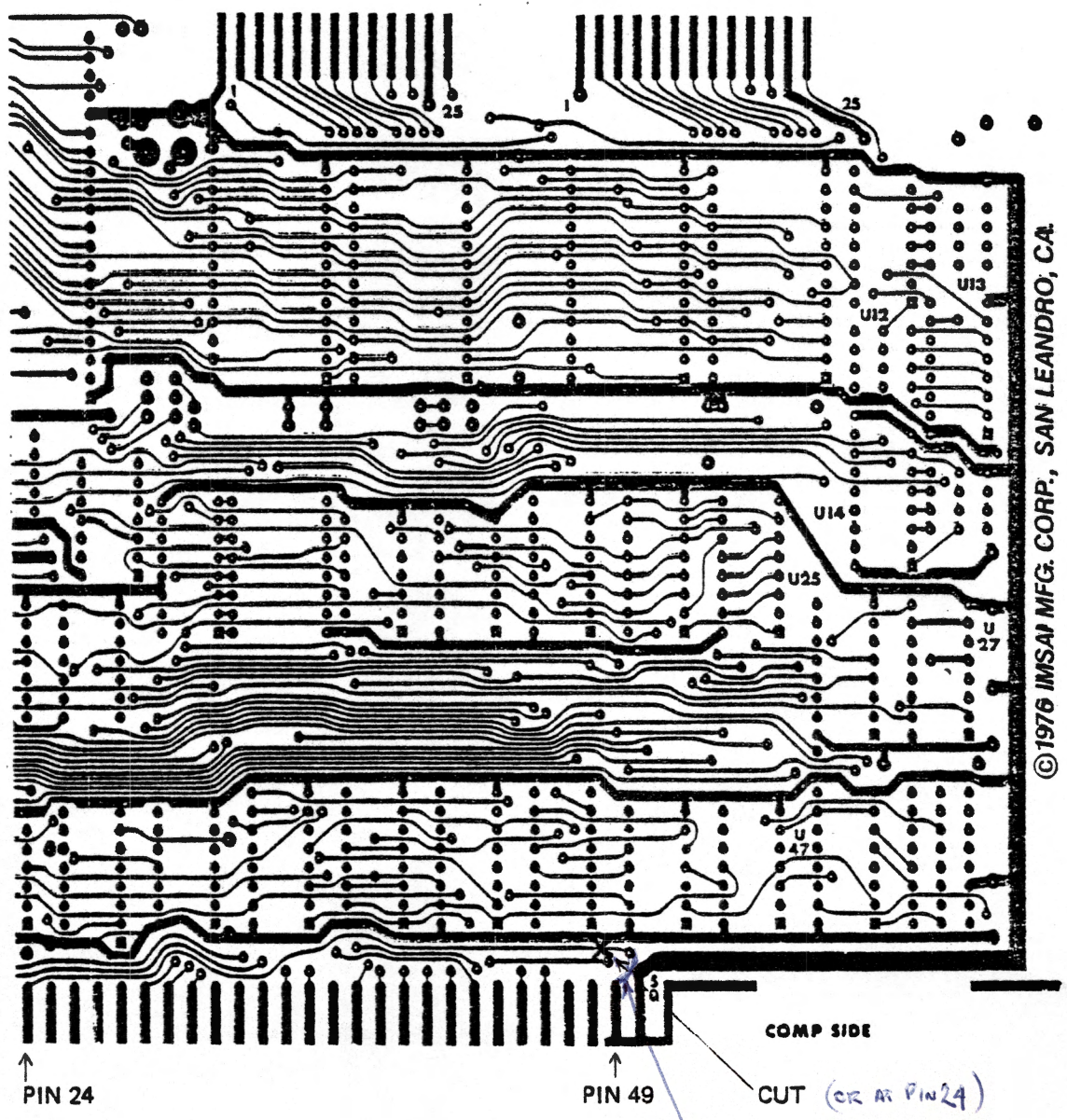
MIO, Rev. 2
Errata
ECO 77-0114
12/19/77

PLEASE NOTE

If you will be using the MIO board in a system with a MPU-B, the following will need to be done. This modification will provide logic timing from the Clock (2ult₃) line (line 49 on the backplane) instead of original ~~Ø~~ line (line 24 on backplane).

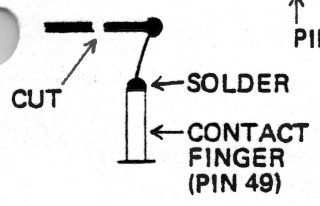
Refer to the diagram when making modifications.

- 1) Cut Ø2 trace (contact pin 24 of J1, to pin 1 of U45) on component side of board at plated-through hole just above contact pin 49 of J1.
- 2) Carefully solder a bare jumper wire between contact pin 49 and plated-through hole, as mentioned above. Do not allow excess solder to flow down onto contact area of contact pin 49.



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DETAIL



PIN 24

PIN 49

COMP SIDE

CUT (OR AT PIN 24)

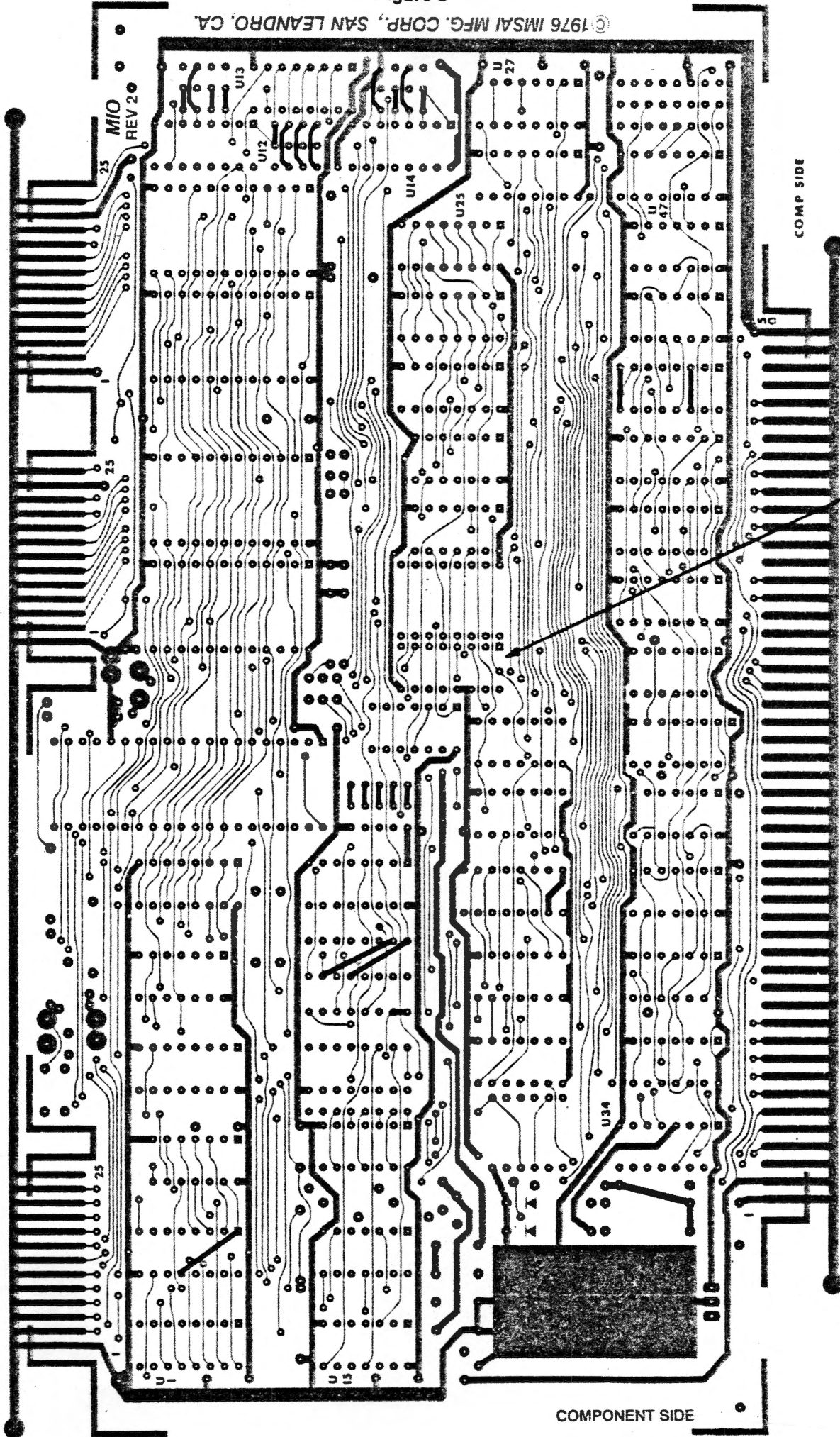
SOLDER

VII.4

JUMPER EXAMPLE ILLUSTRATIONS

Figure 3

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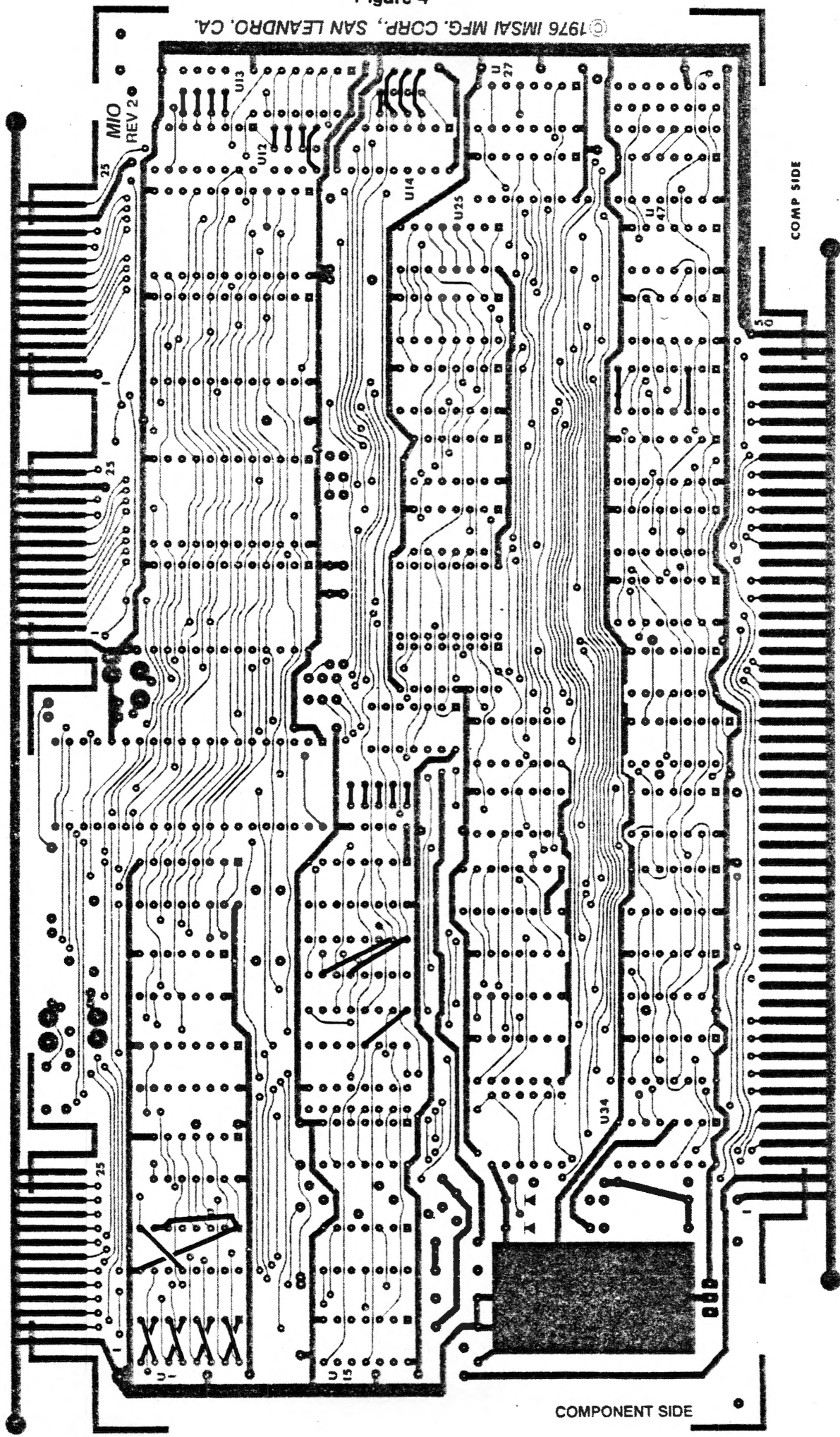


BOARD ADDRESS JUMPERS.
LEAVE OPEN TO PUT BOARD AT BLOCK 0.

TELETYPE

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ECN 77-0011 2/77



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Figure 4

ADM-3
9600 BAUD

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IMSAI MFG. CORP.
SAN LEANDRO, CA.

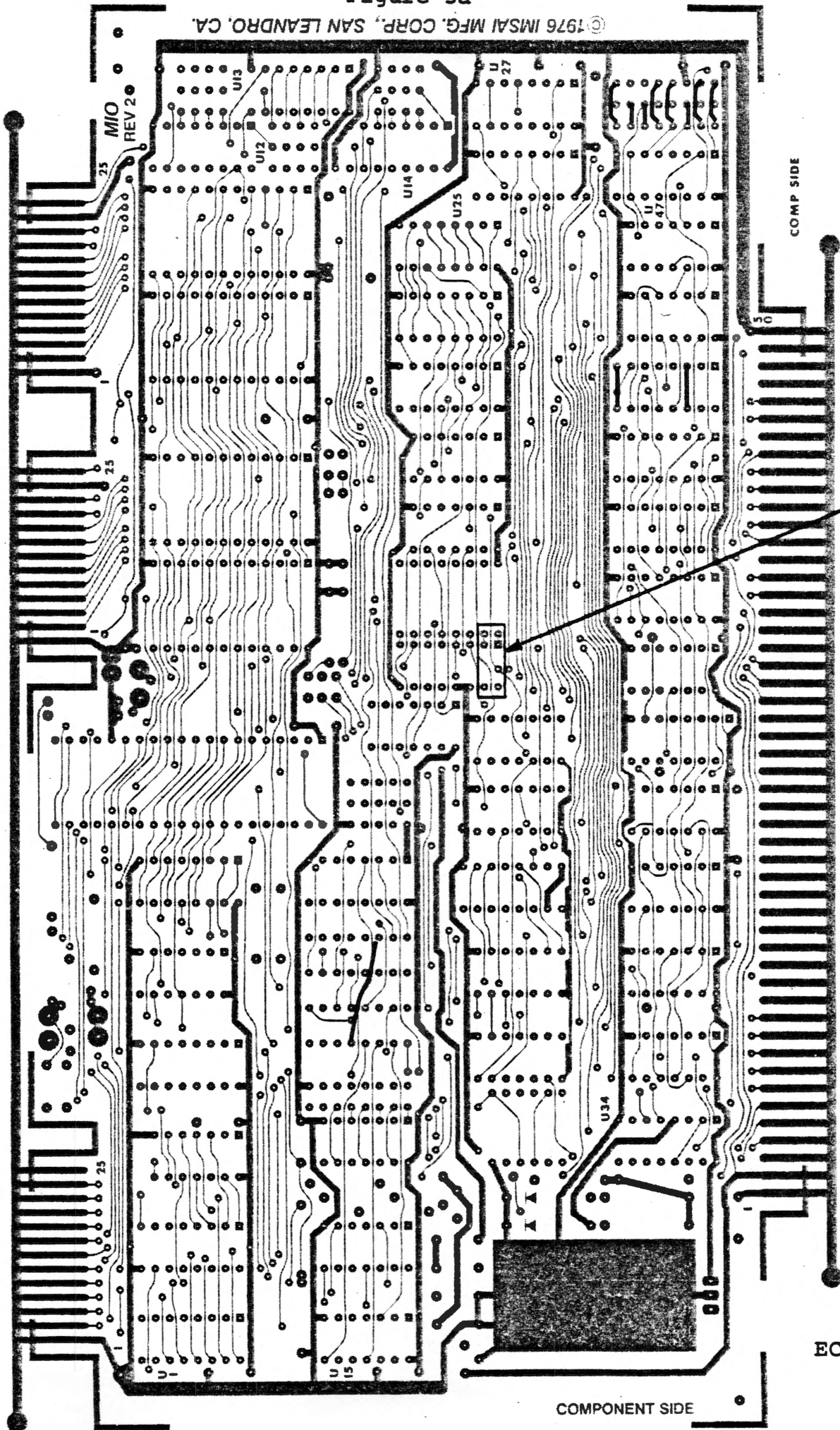
ECN 77-0011 2/77

COMPONENT SIDE

COMP SIDE

Figure 5a

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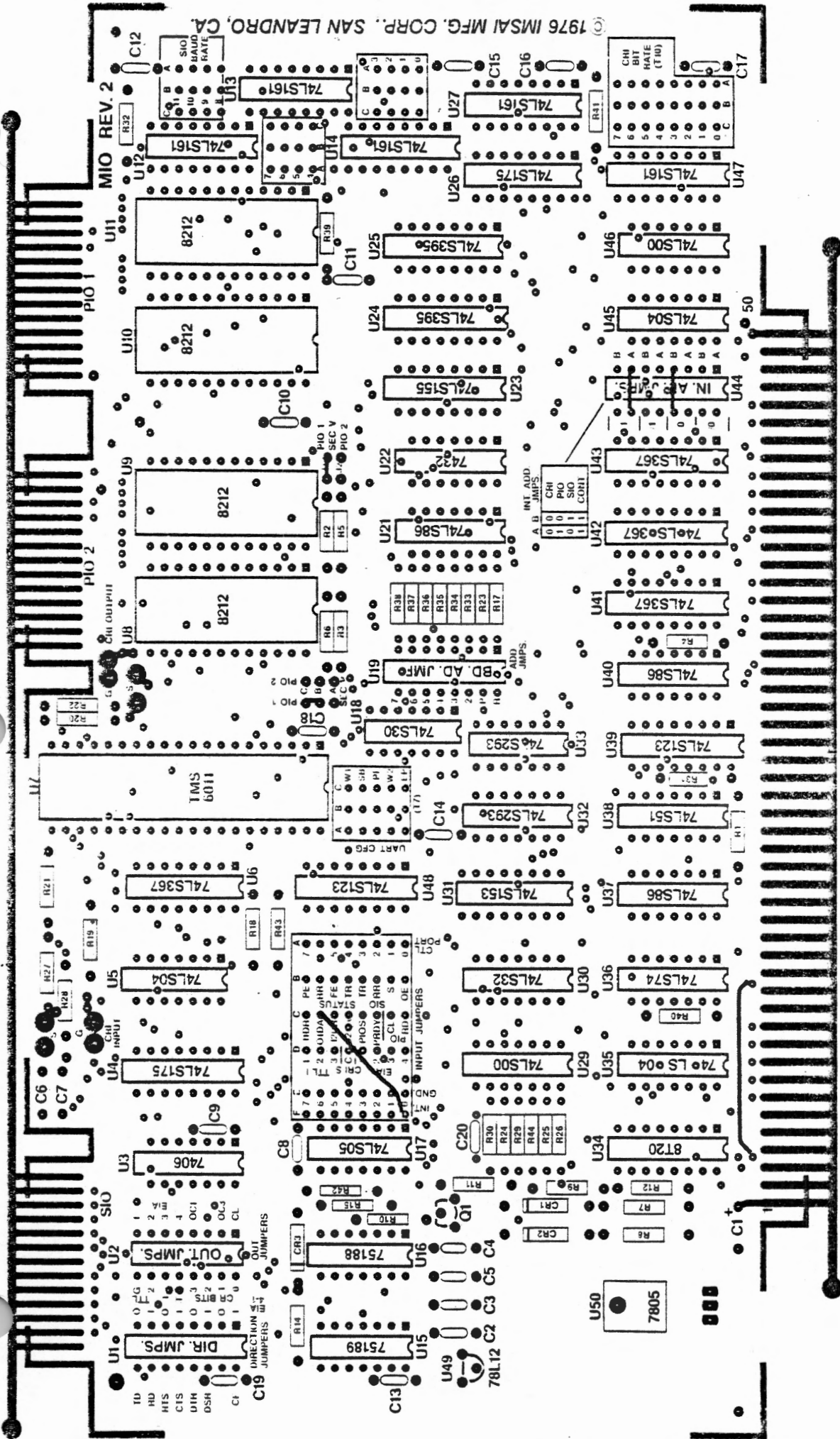


POLARITY SELECT JUMPERS

TARBELL CASSETTE
800 BITS PER SECOND

ECN 77-0014

COMPONENT SIDE



KEY-1 KEYBOARD
NON-VECTORED INTERRUPT MODE

MIO

User Guide

Appendices

APPENDIX A

Test Cassette Description

The Test Cassette contains the programs MIOA and MIOB (the listings of which appear in Appendix B and C, respectively) recorded in standard Tarbell Format at 1500 bits per second plus a sync stream. These programs contain all the test routines described in the User Guide, as well as software handlers for sync generation, block formation, and CRC generation and checking.

The cassette programs are originated to run starting at location 3000 Hex, and they initialize the stack pointer at 3600 Hex. Consequently, 1½ K (1536 bytes) of RAM, starting at 3000, are required to support it.

The test cassette was designed as an aid in debugging and testing the operation of the various ports. The operation of the various functions are described individually in the sections of the User Guide devoted to those ports. It is suggested that, in bringing up an MIO board for the first time, that the CRI interface be tested first. With an operating CRI, the other functions may be tested conveniently by loading the test routines into the computer from the test cassette.

```

;***** MIO TEST CASSETTE LOADER *****
;
; I/O PARAMETERS
;
0040 = CRI EQU 40H ;CASSETTE PORT
0043 = CRL EQU 43H ;CONTROL PORT
0004 = CRY EQU 04H ;CASSETTE READY BIT
;
3800 ORG 3800H
3800 310040 LXI SP,4000H
3803 3E60 MVI A,60H ;SET TO READ BY BIT...
3805 D343 OUT CRL
3807 CD2A38 SYNC: CALL CASIN ;READ 8 BITS
380A FEE6 CPI 0E6H ;IS IT SYNC YET?
380C C20738 JNZ SYNC ;WAIT TILL IT IS
380F 3E20 MVI A,20H ;SET TO READ BY BYTE...
3811 D343 OUT CRL
3813 11B203 LXI D,3B2H ;INIT COUNT
3816 210030 LXI H,3000H ;GET START LOAD ADDRESS
3819 CD2A38 READ: CALL CASIN ;READ A BYTE
381C 77 MOV M,A ;STASH IT...
381D 23 INX H
381E 1B DCX D ;COUNT DOWN
381F 7A MOV A,D ;IS COUNT 0?...
3820 B3 ORA E
3821 C21938 JNZ READ ;CHECK ALL BYTES
3824 2F CMA ;CLEAR LIGHTS...
3825 D3FF OUT 0FFH
3827 C32738 HANG: JMP HANG ;HANG HERE
;
382A DB43 CASIN: IN CRL ;WAIT TILL DATA AVAILABLE...
382C E604 ANI CRY
382E CA2A38 JZ CASIN
3831 DB40 IN CRI ;READ 8 BITS
3833 C9 RET
;
3834 END

```


APPENDIX B
MIOA LISTING

APPENDIX B

```

;MIO BOARD CRI INITIALIZATION PROGRAMS
;ADDRESS DEFINITIONS FOR MIO BOARD CONFIGURED
;AS DEFINED IN MIO USER GUIDE - SECTION 1.2
0042 = SIO EQU 42H
0041 = PIO EQU 41H
0043 = CNT EQU 43H
0040 = CRI EQU 40H
00FF = SSPT EQU 0FFH ;SENSE LIGHTS AND SWITCHES
3100 = BASA EQU 3100H
3000 = BASB EQU 3000H
3600 = BUFR EQU 3600H
3600 = STACK EQU 3600H
3100 = ORG BASA
;JUMP TABLE FOR ENTRY TO MIO TESTS
3100 C31831 JMP SIO1
3103 C33031 JMP SIO2
3106 C34531 JMP SIO3
3109 C31732 JMP PI01
310C C33D32 JMP PI02
310F C34232 JMP PI03
3112 C34732 JMP CRIWT
3115 C36732 JMP CRIRT
;SIO TEST 1 OUTPUT THE VALUE CONTAINED IN THE
; SENSE SWITCHES TO THE SIO PORT. IF AN
; INPUT CHARACTER IS READY AND NO INPUT
; ERRORS OCCUR DISPLAY THE CHARACTER IN
; IN THE SENSE LIGHTS. IF AN INPUT ERROR
; OCCURS, DISPLAY ALL ONES. PAUSE 15
; SECONDS EACH TIME THE SWITCHES ARE CHANGED.
3118 310036 SIO1: LXI SP,STACK
311B AF XRA A ;SET UP CONTROL REG
311C D343 OUT CNT
311E CDE231 SIO11: CALL SSIN ;GET SENSE SWITCHES
3121 CD9E31 CALL SOUT ;OUTPUT CHAR
3124 CDAA31 CALL SINP ;TEST INPUT
3127 CA1831 JZ SIO1 ;IF NO INPUT READY
312A 2F CMA
312B D3FF OUT SSPT ;OUTPUT CHAR OR ERROR FLAG
312D C31E31 JMP SIO11
;SIO TEST 2 READ INPUT CHARACTERS FROM SIO DEVICE
; IF CHARACTER IS READ WITHOUT ERROR,
; OUTPUT CHARACTER TO SIO DEVICE. IF AN
; ERROR OCCURS, IGNORE CHARACTER
3130 310036 SIO2: LXI SP,STACK
3133 AF XRA A ;SET CONTROL REG
3134 D343 OUT CNT
3136 CDAA31 SIO21: CALL SINP ;GET CHAR
3139 CA3631 JZ SIO21 ;NONE READY
313C FA3631 JM SIO21 ;ERROR ON INPUT
313F CD9E31 CALL SOUT ;OUTPUT VALID CHAR
3142 C33631 JMP SIO21
;SIO TEST 3 CONTINUOUSLY TRANSMIT ALL POSSIBLE BIT
; PATTERS MASKED WITH THE COMPLEMENT OF THE
; SENSE SWITCHES. CHECK FOR RECEIVE ERRORS
; AND DISPLAY 0FFH IF ANY OCCUR FOLLOWED BY
; STATUS WITH PE,OE,FE,RRDY AND TRDY IN BITS

```

```

;          4 TO 0 RESPECTIVELY. COMPARE RECEIVED CHAR
;          WITH TRANSMITTED CHAR. DISPLAY OFEH IF DIFFERENT
;          FOLLOWED BY TRANSMITTED CHAR AND
;          RECEIVED CHAR. IN NORMAL OPERATION DISPLAY
;          TRANSMITTED CHAR.
3145 310036 SIO3: LXI SP,STACK
3148 AF      XRA A          ;SET CONTROL
3149 D343    OUT CNT
314B 0E00    MVI C,0          ;ORIGINAL CHAR VALUE
314D DBFF    SIO31: IN SSPT      ;GET ORIGINAL SENSE SWITCH
314F 32FA31  STA SSV         ;FORM CHAR
3152 2F      CMA          ;FORM CHAR
3153 A1      ANA C
3154 0C      INR C          ;SET NEXT VALUE
3155 57      MOV D,A        ;SAVE IT FOR COMPARE
3156 2F      CMA          ;FOR PROPER LIGHTS
3157 D3FF    OUT SSPT      ;DISPLAY IT
3159 2F      CMA          ;FOR PROPER VALUE
315A CD9E31  CALL SOUT         ;OUTPUT IT
315D CDA331  SIO32: CALL SINP        ;TEST INPUT
3160 CA5D31  JZ SIO32       ;IF NONE READY
3163 FA8131  JM SIO33       ;ON ERROR
3166 5F      MOV E,A        ;MASK INPUT
3167 3AFA31  LDA SSV
316A 2F      CMA
316B A3      ANA E
316C BA      CMP D          ;COMPARE WITH OUTPUT
316D CA4D31  JZ SIO31       ;RELOOP IF OK
3170 5F      MOV E,A
3171 3EFE    MVI A,0FEH     ;ERROR FLAG
3173 CD8E31  CALL DISP        ;DISPLAY TILL SENSE SWITCHES CHANGE
3176 7A      MOV A,D        ;TRANS CHAR
3177 CD8E31  CALL DISP
317A 7B      MOV A,E        ;RECEIVED CHAR
317B CD8E31  CALL DISP
317E C34D31  JMP SIO31
3181 57      SIO33: MOV D,A        ;SAVE ERRORS
3182 3EFE    MVI A,0FEH     ;ERROR FLAG
3184 CD8E31  CALL DISP
3187 7A      MOV A,D        ;STATUS RESULTS
3188 CD8E31  CALL DISP
318B C34D31  JMP SIO31
;GENERAL UTILITY ROUTINES FOR SIO TEST.
;THIS ROUTINE DISPLAYS THE VALUE IN A UNTIL
;SENSE SWITCHES ARE CHANGED.
318E 2F      DISP: CMA          ;FOR PROPER LIGHTS
318F D3FF    OUT SSPT
3191 DBFF    IN SSPT        ;INITIAL SENSE SWITCHES
3193 47      MOV B,A
3194 CDFB31  CALL DLAS        ;WAIT A WHILE
3197 DBFF    DIS1: IN SSPT      ;NEW VALUE?
3199 A8      XRA B
319A CA9731  JZ DIS1 ;WAIT FOR DIFFERENCE
319D C9      RET
;OUTPUT CHARACTER IN A WHEN DEVICE READY.
319E 47      SOUT: MOV B,A        ;WAIT TIL READY
319F DB43    SOUT1: IN CNT
31A1 E601    ANI 1

```

```

31A3 CA9F31      JZ SOUT1
31A6 78          MOV A,B
31A7 D342       OUT SIO          ;CHAR OUT
31A9 C9         RET
;INPUT A CHAR WHEN READY. IF AN ERROR
;OCCURS, PUT PE,OE,FE,RRDY,TRDY IN 4 TO 0.
31AA DB43      SINP: IN CNT          ;SEE IF READY ON ERROR
31AC E60A      ANI 0AH
31AE C8        RZ
31AF EE0A      XRI 0AH          ;YES, TEST ERROR
31B1 CABA31    JZ SIN1
31B4 EE02      XRI 2           ;SEE IF OLD ERROR FLAG
31B6 C8        RZ             ;IF SO, RETURN
31B7 DB42      IN SIO         ;NO ERROR, GET CHAR
31B9 C9        RET
31BA 3E80      SIN1: MVI A,80H   ;GET ERROR BITS
31BC D343      OUT CNT        ;PARITY ERROR
31BE DB43      IN CNT
31C0 E608      ANI 8
31C2 07        RLC
31C3 47        MOV B,A
31C4 3EC0      MVI A,0C0H     ;FRAMING ERROR
31C6 D343      OUT CNT
31C8 DB43      IN CNT
31CA E608      ANI 8
31CC 0F        RRC
31CD 80        ADD B
31CE 47        MOV B,A
31CF 3E40      MVI A,40H     ;OVERUN,RRDY AND TRDY
31D1 D343      OUT CNT
31D3 DB43      IN CNT
31D5 E60B      ANI 0BH
31D7 80        ADD B
31D8 47        MOV B,A
31D9 DB42      IN SIO         ;CLEAR CHARACTER
31DB AF        XRA A          ;RESET CONTROL FOR ERROR FLAG
31DC D343      OUT CNT
31DE F680      ORI 80H
31E0 78        MOV A,B
31E1 C9        RET
;INPUT SENSE SWITCHES-DELAY IF DIFFERENT
31E2 DBFF      SSIN: IN SSPT     ;GET THEM
31E4 47        MOV B,A
31E5 3AFA31    LDA SSAV        ;COMPARE WITH PAST
31E8 A8        XRA B
31E9 78        MOV A,B
31EA C8        RZ
31EB CDFB31    CALL DLA5        ;DIFFERENT WAIT FOR A WHILE
31EE CDFB31    CALL DLA5
31F1 CDFB31    CALL DLA5
31F4 DBFF      IN SSPT        ;GET NEW VALUE
31F6 32FA31    STA SSAV
31F9 C9        RET
31FA 00        SSAV: DB 0
;DELAY 5 SECONDS - REQUIRES 10 MILLION CYCLES (APPROXIMATELY)
31FB 3E00      DLA5: MVI A,0
31FD 0EC9      MVI C,201
31FF CD0B32    DLA51: CALL DONE

```

```

3202 0C          INR C
3203 C2FF31     JNZ DLA51
3206 3C          INR A
3207 C2FF31     JNZ DLA51
320A C9          RET
320B E5         DONE:  PUSH H          ;TAKE 121 CYCLES
320C E1         POP H
320D E5         PUSH H
320E E1         POP H
320F E5         PUSH H
3210 E1         POP H
3211 E5         PUSH H
3212 E1         POP H
3213 E5         PUSH H
3214 E1         POP H
3215 7F         MOV A,A
3216 C9          RET

;PIO TEST 1     READ SENSE SWITCHES AND OUTPUT
;              TO BOTH PORTS.
3217 0E01     PIO1:  MVI C,1          ;SET TEST 1 FLAG
3219 DBFF     PIO11: IN SSPT         ;GET VALUE
321B 2F         PIO12: CMA           ;FOR PROPER LIGHTS
321C D3FF     OUT SSPT             ;OUTPUT TO LIGHTS
321E 2F         CMA               ;FOR PROGRAM USE
321F 47         MOV B,A
3220 AF         XRA A              ;SET FOR PORT 1
3221 D343     OUT CNT
3223 78         MOV A,B
3224 D341     OUT PIO
3226 3E80     MVI A,80H           ;NOW FOR PORT 2
3228 D343     OUT CNT
322A 78         MOV A,B
322B D341     OUT PIO
322D 0C         INR C              ;SEE WHICH TEST IT IS
322E 0D         DCR C
322F FA3532     JM PIO13
3232 C21932     JNZ PIO11
3235 79         PIO13: MOV A,C      ;TEST 2 OR 3
3236 D343     OUT CNT             ;SET TO READ PROPER INPUT PORT
3238 DB41     IN PIO
323A C31E32     JMP PIO12

;PIO TEST 2     READ PIO PORT 1 AND OUTPUT
;              TO PORTS 1 AND 2 AND SENSE LIGHTS
323D 0E00     PIO2:  MVI C,0        ;FLAG FOR PORT 1 IN
323F C33532     JMP PIO13

;PIO TEST 3     READ PIO PORT 2 AND OUTPUT
;              TO PORTS 1 AND 2 AND SENSE LIGHTS.
3242 0E80     PIO3:  MVI C,80H     ;FLAG FOR PORT 2 IN
3244 C33532     JMP PIO13

;CRI WRITE TEST WRITE A BLOCK OF 256 BYTES
;              WITH EACH BYTE CONTAINING ITS ADDRESS
;              WITHIN THE BLOCK.
3247 310036     CRIWT: LXI SP,STACK
324A 210036     LXI H,BUFR        ;FILL BUFFER WITH ADDRESS
324D AF         XRA A
324E 77         CRIW1: MOV M,A
324F 23         INX H
3250 3C         INR A

```

```

3251 C24E32      JNZ CRIW1
3254 210036      LXI H,BUFR      ;SET PARAMATERS
3257 1E00        MVI E,0          ;256 BYTES
3259 3E3F        MVI A,3FH
325B D3FF        OUT SSPT      ;GIVE LBGHTS AN INITIAL VALUE
325D CD9E32      CALL WRIT       ;DO THE WRITE
3260 AF          CRIW2: XRA A      ;ALL DONE LOOP
3261 2F          CMA          ;FOR PROPER LIGHTS
3262 D3FF        OUT SSPT
3264 C36032      JMP CRIW2

;CRI READ TEST      READ A BLOCK OF 256 BYTES.
;                   CHECK THAT EACH BYTE CONTAINS ITS ADDRESS
;                   WITHIN THE BLOCK.  CRC ERROR IS ALSO DETECTED BY
;                   READ HANDLER.

3267 310036      CRIRT: LXI SP,STACK
326A 210036      LXI H,BUFR      ;SET PARAMATERS
326D 1E00        MVI E,0          ;256 BYTES
326F 3E3F        MVI A,3FH      ;INITIAL VALUE FOR LIGHTS
3271 D3FF        OUT SSPT
3273 CD0133      CALL READ       ;READ THE BLOCK
3276 CA7E32      JZ CRI1      ;JUMP IF NO CRC ERROR
3279 3EFF        MVI A,OFFH     ;ELSE,DISPLAY IT
327B CD8E31      CALL DISP
327E 1E00        CRIR1: MVI E,0      ;DO A BYTE BY BYTE COMPARE
3280 210036      LXI H,BUFR
3283 7E          CRIR3: MOV A,M
3284 BB          CMP E          ;COMPARE A BYTE
3285 CA9532      JZ CRIR2
3288 3EFE        MVI A,0FEH     ;DISPLAY THE ERROR
328A CD8E31      CALL DISP
328D 7B          MOV A,E          ;CORRECT VALUE
328E CD8E31      CALL DISP
3291 7E          MOV A,M          ;ACTUAL VALUE
3292 CD8E31      CALL DISP
3295 23          CRIR2: INX H
3296 1C          INR E          ;LOOP COUNT
3297 C28332      JNZ CRIR3
329A C36032      JMP CRIW2      ;IF ALL DONE

;GENERAL HANDLERS FOR TARBELL OR BYTE/LANCASTER ON
;CRI.  USE 1-255 BYTE BLOCK AND STANDARD CRC ROUTINE
;FOR ERROR CHECKING.
329D 00          TYPF: DB 0      ;SET 0 FOR TARBELL, NONZERO FOR BYTE/LANCASTER
;WRITE ROUTINE - THE FOLLOWING PARAMATERS ARE EXPECTED ON ENTRY
;                   HL - CONTAIN THE MEMORY LOCATION FOR THE BLOCK
;                   E - CONTAINS THE BLOCK SIZE, 1-256. (0=256)

329E 3E10        WRIT: MVI A,10H
32A0 D343        OUT CNT
32A2 D340        OUT CRI      ;RESET BYTE COUNTER
32A4 3E3C        MVI A,03CH     ;START BYTE
32A6 CDCB32      CALL WRBYT     ;OUTPUT IT
32A9 3EE6        MVI A,0E6H     ;SYNC BYTE
32AB CDCB32      CALL WRBYT     ;WRITE A BYTE WHEN READY
32AE 01FFFF      LXI B,0FFFFH    ;INITIALIZE CRC VALUE
32B1 7E          WRIT1: MOV A,M      ;GET A BYTE
32B2 CD8F33      CALL CRC      ;ADD TO CRC
32B5 7E          MOV A,M      ;GET THE BYTE AGAIN
32B6 CDCB32      CALL WRBYT     ;WRITE IT WHEN READY
32B9 23          INX H

```

```

32BA 1D          DCR E          ;LOOP COUNT
32BB C2B132     JNZ WRIT1     ;LOOP TIL DONE
32BE 78          MOV A,B       ;WRITE CRC BYTE 1
32BF CDCB32     CALL WRBYT
32C2 79          MOV A,C       ;BYTE 2
32C3 CDCB32     CALL WRBYT
32C6 AF          XRA A          ;TRAILING ZERO BYTE
32C7 CDCB32     CALL WRBYT
32CA C9          RET
32CB 57          WRBYT: MOV D,A     ;SAVE THE BYTE
32CC DB43       WRBY2: IN CNT     ;WAIT TIL READY
32CE E604        ANI 4
32D0 CACC32     JZ WRBY2
32D3 3A9D32     LDA TYPF     ;SEE WHICH TYPE
32D6 A7          ANA A
32D7 C2DE32     JNZ WRBY3
32DA 7A          MOV A,D       ;TARBELL
32DB D340        OUT CRI
32DD C9          RET
32DE E5          WRBY3: PUSH H     ;BYTE/LANCASTER-SERIALIZE BYTE
32DF 2608        MVI H,8
32E1 CDF432     WRBY7: CALL WRBYS    ;WRITE A BIT
32E4 25          DCR H       ;BIT COUNTER
32E5 C2EA32     JNZ WRBY6
32E8 E1          POP H       ;DONE, RESTORE H
32E9 C9          RET
32EA DB43       WRBY6: IN CNT
32EC E504        ANI 4
32EE CAEA32     JZ WRBY6
32F1 C3E132     JMP WRBY7
32F4 7A          WRBYS: MOV A,D
32F5 17          RAL
32F6 57          MOV D,A     ;CARRY HAS FIRST BIT
32F7 3EFF        MVI A,0FFH   ;FOR A ONE
32F9 DAFE32     JC WRBY4
32FC 3EAA        MVI A,0AAH   ;FOR A ZERO
32FE D340        WRBY4: OUT CRI
3300 C9          RET
;READ ROUTINE READS IN TARBELL OR BYTE/LANCASTER AS
;A FUNCTION OF TYPF. INPUT PARAMATERS ARE:
; HL - CONTAIN ADDRESS OF INPUT BUFFER
; E - CONTAINS BLOCK SIZE, 1-256 (0=256)
;RETURNS WITH ZERO FLAG SET OF NO CRC ERROR OCCURS
3301 3E60        READ: MVI A,60H ;SET TO RECOGNIZE SYNC
3303 D343        OUT CNT
3305 CD3233     CALL RBSN    ;SYNC ON BYTE BASIS OF BYTE/LANCASTER
3308 CD5633     READ1: CALL GBIT ;GET BYTE ON NEXT SHIFT
330B FEE6        CPI 0E6H   ;SEE IF SYNC
330D C20833     JNZ READ1
3310 3E20        MVI A,20H   ;OKAY, GO TO BYTE READY
3312 D343        OUT CNT
3314 01FFFF     LXI B,0FFFFH ;SET INITIAL CRC VALUE
3317 CD6A33     READ2: CALL GBYT ;GET AA BYTE
331A 77          MOV M,A ;STORE IT
331B CD8F33     CALL CRC    ;ADD TO CRC
331E 23          INX H
331F 1D          DCR E       ;LOOP COUNT
3320 C21733     JNZ READ2

```

```

3323 CD6A33      CALL GBYT      ;CRC BYTE 1
3326 CD8F33      CALL CRC      ;FORM VALUE
3329 CD6A33      CALL GBYT      ;BYTE 2
332C CD8F33      CALL CRC      ;FOR THE LAST TIME!
332F 79          MOV A,C      ;SET FLAG
3330 B0          ORA B
3331 C9          RET
3332 3A9D32      RBSN: LDA TYPF      ;SYNC IF REQUIRED
3335 A7          ANA A
3336 C8          RZ
3337 1600        MVI D,0      ;SET FOR BIT SYNC RECOGNITION
3339 CD4C33      RBS2: CALL RBS1      ;NOW WAIT FOR A ZERO BIT FOLLOWED
333C 17          RAL      ;BY EIGHT ONES SO HAVE
333D DA3933      JC RBS2      ;TARBELL BYTE SAME AS LANCASTER BIT.
3340 CD4C33      CALL RBS1      ;HAVE A ZERO LOOK FOR ONES
3343 3C          INR A
3344 C23933      JNZ RBS2
3347 3E20        MVI A,20H
3349 D343      OUT CNT
334B C9          RET      ;ALL SET, SET TO GET BYTES FROM NOW ON
334C DB43      RBS1: IN CNT
334E E604      ANI 4
3350 CA4C33      JZ RBS1
3353 DB40      IN CRI
3355 C9          RET
3356 DB43      GBIT: IN CNT      ;GET BYTE AFTER NEXT BIT SHIFT
3358 E604      ANI 4
335A CA5633      JZ GBIT
335D 3A9D32      LDA TYPF
3360 A7          ANA A
3361 DB40      IN CRI
3363 C8          RZ      ;RETURN ON TARBELL
3364 C601      ADI 1      ;CONVERT TO 1 OR 0 BIT
3366 7A          MOV A,D
3367 17          RAL      ;ADD TO BYTE
3368 57          MOV D,A
3369 C9          RET
336A DB43      GBYT: IN CNT      ;WAIT TIL READY
336C E604      ANI 4
336E CA6A33      JZ GBYT
3371 3A9D32      LDA TYPF      ;CHECK MODE
3374 A7          ANA A
3375 C27B33      JNZ GBYT1
3378 DB40      IN CRI      ;TARBELL, JUST READ BYTE
337A C9          RET
337B E5          GBYT1: PUSH H      ;LANCASTER NEED TO ASSEMBLE A BYTE
337C 2607        MVI H,7
337E DB40      IN CRI      ;FIRST BIT
3380 57          MOV D,A
3381 CD4C33      GBYT2: CALL RBS1      ;GET NEXT TARBELL BYTE=LANCASTER BIT
3384 C601      ADI 1
3386 7A          MOV A,D
3387 17          RAL
3388 57          MOV D,A ;ADD TO BYTE
3389 25          DCR H
338A C28133      JNZ GBYT2
338D E1          POP H
338E C9          RET

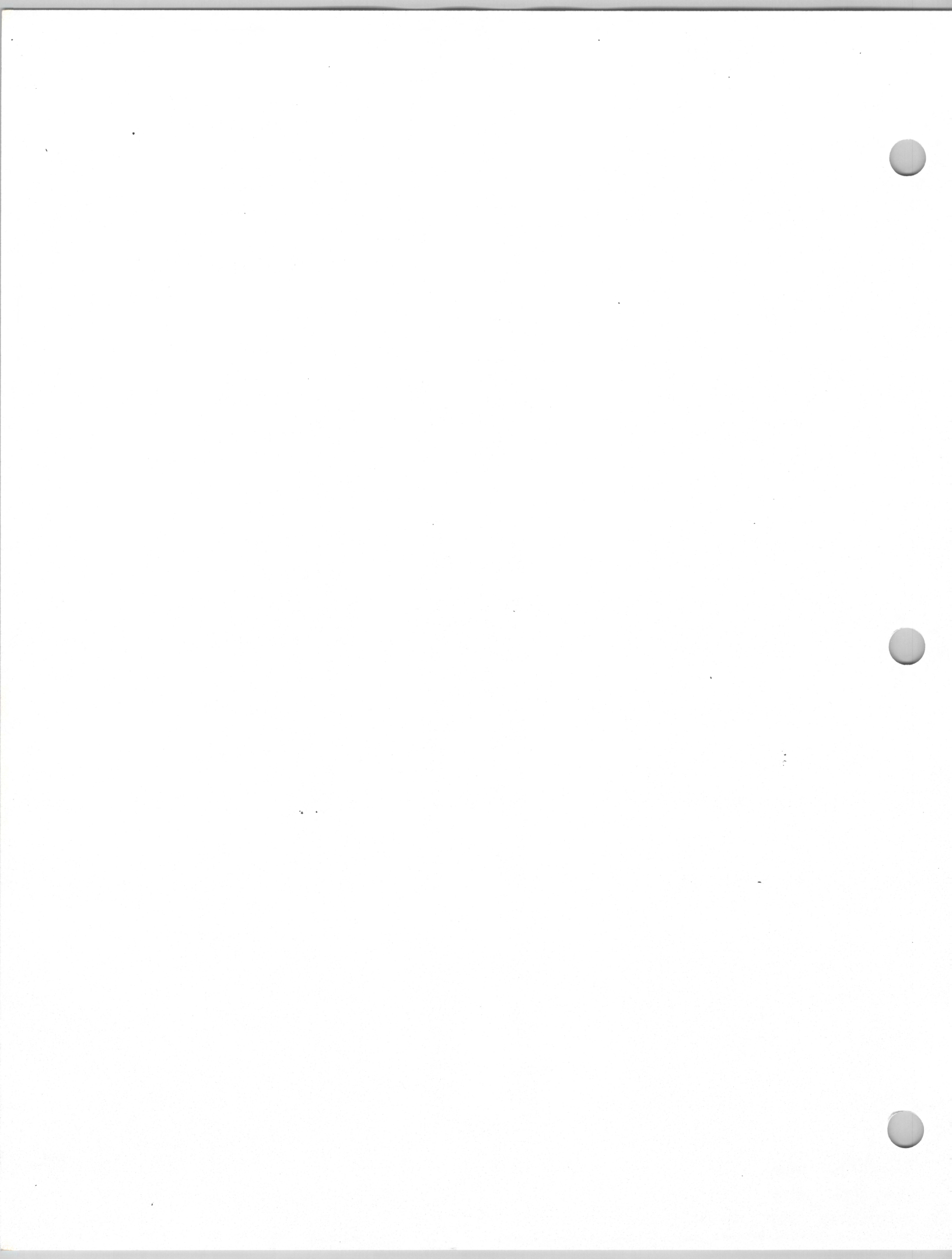
```



```
          ;GENERAL CRC ROUTINE.  COMPUTE FOR ONE BYTE
CRC:      PUSH H
          PUSH D
          XRA B
          MOV H,A
          RLC
          RLC
          RLC
          RLC
          XRA H
          MOV L,A
          ANI 0F0H
          MOV D,A
          ADD L
          MOV E,A
          MOV A,D
          339F CE00  ACI 0
          33A1 A9    XRA C
          33A2 47    MOV B,A
          33A3 7C    MOV A,H
          33A4 E6F0  ANI 0F0H
          33A6 67    MOV H,A
          33A7 AB    XRA E
          33A8 4F    MOV C,A
          33A9 7C    MOV A,H
          33AA 0F    RRC
          33AB 0F    RRC
          33AC 0F    RRC
          33AD A8    XRA B
          33AE 47    MOV B,A
          33AF D1    POP D
          33B0 E1    POP H
          33B1 C9    RET
          33B2      END
```

APPENDIX C

MIOB LISTING



APPENDIX C

```

;MIO BOARD CRI INITIALIZATION PROGRAMS
;ADDRESS DEFINITIONS FOR MIO BOARD CONFIGURED
;AS DEFINED IN MIO USER GUIDE - SECTION I.2
0042 =      SIC      EQU 42H
0041 =      PIO      EQU 41H
0043 =      CNT      EQU 43H
0040 =      CRI      EQU 40H
00FF =      SSPT     EQU 0FFH      ;SENSE LIGHTS AND SWITCHES
3100 =      BASA     EQU 3100H
3000 =      BASB     EQU 3000H
3600 =      BUFR     EQU 3600H
3600 =      STACK    EQU 3600H
;SYNC RECOGNITION PROGRAM - FINDS INITIAL SYNC
;AND THEN SETS ALL SENSE LIGHTS FOR EACH SYNC
;BYTE THEREAFTER.  IF A SYNC BYTE IS MISSED SETS SENSE
;SENSE SWITCHES TO ZERO AND LOOKS FOR SYNC AGAIN.
3000          ORG BASB
3000 3E60      SYNRR: MVI A,60H
3002 D343      OUT CNT          ;ENABLE READ AND READY BY BIT
3004 AF        XRA A
3005 2F        CMA              ;FOR PROPER LIGHTS
3006 D3FF      OUT SSPT        ;CLEAR LIGHTS
3008 DB43      SYNRL: IN CNT     ;WAIT FOR READY
300A E604      ANI 4
300C CA0830    JZ SYNRL
300F DB40      IN CRI          ;SEE IF SYNC BYTE
3011 D6E6      SUI 0E6H
3013 C20030    JNZ SYNRR       ;IF NOT, RELOOP
3016 D3FF      OUT SSPT        ;YES SET LIGHTS TO ONES
3018 3E20      MVI A,20H      ;SET TO READ BYTES
301A D343      OUT CNT
301C C30830    JMP SYNRL       ;GO LOOK AT NEXT BYTE
;SYNC GENERATION PROGRAM - WRITES SYNC BYTE CONTINUOUSLY
301F 3E10      SYNG: MVI A,10H ;SET WRITE ENABLE
3021 D343      OUT CNT
3023 3EE6      SYNG2: MVI A,0E6H ;OUTPUT SYNC CHAR
3025 D340      OUT CRI
3027 DB43      SYNG1: IN CNT    ;WAIT TIL READY AGAIN
3029 E604      ANI 4
302B CA2730    JZ SYNG1
302E C32330    JMP SYNG2       ;THEN DO ANOTHER
;BOOTSTRAP PROGRAM FOR TARBELL CODE
3031 210031    BOOT: LXI H,BASA ;GET STARTING ADDRESS
3034 3E60      MVI A,60H      ;SET READ AND READY BY BIT
3036 D343      OUT CNT
3038 DB43      BOOT1: IN CNT   ;LOOK FOR SYNC CHAR
303A E604      ANI 4
303C CA3830    JZ BOOT1
303F DB40      IN CRI        ;GET CHAR
3041 FEE6      CPI 0E6H
3043 C23830    JNZ BOOT1
3046 3E20      MVI A,20H      ;GO TO BYTE
3048 D343      OUT CNT
304A DB43      BOOT2: IN CNT   ;WAIT FOR BYTE
304C E604      ANI 4
304E CA4A30    JZ BOOT2

```

```
3051 DB40          IN CRI          ;GET IT
3053 77           MOV M,A ;STORE IT
3054 23           INX H
3055 C34A30       JMP BOOT2          ;GET NEXT BYTE
;DUMP PROGRAM FOR FORMING TAPE FOR LATER REBOOT
3058 210031       DUMP: LXI H,BASA
305B 3E10         MVI A,10H
305D D343         OUT CNT          ;SET CONTROL FOR WRITE
305F D340         OUT CRI          ;TO CLEAR COUNTERS
3061 DB43         DUMP1: IN CNT      ;WAIT UNTIL READY
3063 E604         ANI 4
3065 CA6130       JZ DUMP1
3068 3E3C         MVI A,03CH
306A D340         OUT CRI          ;WRITE START CHARACTER
306C 06E6         MVI B,0E6H       ;SYNC CHARACTER
306E DB43         DUMP2: IN CNT      ;WAIT UNTIL READY
3070 E604         ANI 4
3072 CA6E30       JZ DUMP2
3075 78           MOV A,B          ;GET CHARACTER
3076 D340         OUT CRI          ;WRITE IT
3078 46           MOV B,M          ;NEXT CHARACTER
3079 23           INX H
307A C36E30       JMP DUMP2
307D              END
```

APPENDIX D

DEBUGGING INFORMATION

SOME HINTS ON DEBUGGING

If, after assembling the board, a problem occurs, there are a number of basic things to check for.

1. CAREFULLY CHECK THE BOARD FOR CORRECT PLACEMENT AND ORIENTATION OF ALL COMPONENTS. Use the Assembly Drawing as a guide. Many problems occur because of a misplaced component on the board.
 - ... Check the positioning of all capacitors.
 - ... Check the placement of all resistors.
 - ... Check all chips for correct placement and orientation. Be sure pin 1 on all chips are as shown on the Assembly Drawing. Note that pin 1 of every chip faces down, toward the bottom of the board.
2. CAREFULLY CHECK THE SOLDER SIDE OF THE BOARD FOR ANY SOLDER CROSSES OR BAD SOLDER JOINTS. This is best done under a bright light. The majority of all problems found are due to a single solder cross or short.
3. CAREFULLY CHECK THE POSITIONING OF ALL BOARD OPTION JUMPERS. Use the MIO User Guide as a reference.
4. CHECK ALL SUPPLY VOLTAGE LEVELS. Many times a regulator or diode is defective and simply provides insufficient voltage levels. The MIO board uses 4 separate voltages.
 - ... +5 volts Check the output of the 7805 with respect to ground.
 - ...+12 volts Check the output of the 78L12 with respect to ground.
 - ...-12 volts Check the cathode of CR1 with respect to ground.
 - ... -5 volts Check the cathode of CR2 with respect to ground.

Before proceeding, double check all external connections to I/O devices. Make sure that all I/O pins are connected as explained in the User Guide. Note that the board edge connector numbers are not the same as the EIA 25-pin connector numbers.

MIO
Debugging Information

If the problem still persists, it will be necessary to use the MIO Schematic Drawing as a guide in troubleshooting. While it may seem very complex at first glance, it is much easier to understand once it has been broken down into FUNCTIONAL BLOCKS (e.g., Board Enable Circuits, SIO Port Circuits, CRI Port Circuits, PIO Port Circuits, Control Port Circuits, Input Receivers, Output Drivers, etc.).

The User is encouraged to familiarize him/herself with the Schematic Drawings if s/he is to do any further debugging.

1. The first step in debugging is to narrow down the problem as specifically as possible.
EXAMPLE: If the SIO Test fails, does it fail in Transmit or Receive mode? If it fails only in Transmit mode, does it fail for all characters or just one in particular? How does it fail? Is a bit being dropped, or is any input being received at all? Etc.

TRY TO WORK ON ONE SPECIFIC PROBLEM AT A TIME.

2. Armed with this information, the User should use the following reference sources to understand the logic flow for the operation which fails (determined in Step 1 above).
 1. Schematic Drawing;
 2. Theory of Operation Chapter;
 3. A reference such as the TTL DATA BOOK; and
 4. Test Program Listings.
3. Follow the Logic Flow, determined in Step 2, above, by checking circuit points with an Oscilloscope or Logic Probe. It is usually easier to start checking at the logical endpoint and work back towards the source.

You will be looking for:

1. incorrect signal levels;
2. missing signals;
3. incorrect voltage levels of signals; and
4. signals which occur at the wrong time.

Once an inconsistency or problem has been located, trace back towards the source of the signal to locate the source of the problem.

MIO
Debugging Information

The problem can usually be traced to:

1. a defective chip;
2. a solder cross or bad solder joint or
3. a misplaced or incorrectly oriented component.

A BRIEF LIST OF PROBLEMS WITH SUGGESTED POINTS TO CHECK ARE GIVEN BELOW.

NONE OF THE PORTS RESPOND

1. Check the jumpering of the EXTERNAL ADDRESS JUMPER AREA.
2. Check the Board Enable Circuits. U18-8 goes low when the processor executes an output instruction to the MIO Board Addrsss.

ONE OF THE PORTS DOES NOT RESPOND

1. Check the jumpering of the Internal Address Jumper Area.
2. Check U23: The outputs of U23 are the Internal Port Select Signals. There are four Register Load Signals and four Read Enables.

NO INPUT FROM ANY INPUT PORTS

1. Check the Input Bus Drivers U42 and U43. Check for Enables U43-1, U43-15, and U42-15, going low.

NO OUTPUT TO ANY OUTPUT PORT

1. Check the Output Bus Drivers U41 and U42. Check for Enables U42-1 and U41-1 going low.

SIO PORTS

NO OUTPUT FROM SIO TO EXTERNAL DEVICE

1. Check U7-25 UART Transmit Data Line. If Data is present here, carefully check the jumpering of the OJA and/or OJA Line Drivers.

If Data is not present, check SIO Configuration Jumpers and check all Control Inputs to the UART U7 (especially U7-23, UART Data Load).

NO INPUT FROM EXTERNAL DEVICE TO SIO

1. Check U7-20, the UART Receive Data Line.
If Data is not present here, carefully check the jumpering of the IJA and/or the IJA Receivers.

If Data is present, check the SIO Configuration Jumpers and check all Control Inputs to the UART U7 (especially U7-4, UART Read Enable).

PIO PORTS

NO INPUT FROM PIO INPUT PORTS

1. Check the STB from the external device. It should set /INT low.
2. Check the jumpering of the PIO Strobe Select.
3. Check the jumpering of the IJA.
4. Check the PIO Port enable (/DS1) (DS2).
It is active when the Processor reads the Port. /INT should be reset to a high at this time.

NO OUTPUT TO PIO OUTPUT PORTS

1. Check the OCDR Line from the external device.
It should set /INT Low.
2. Check the jumpering of the IJA.
3. Check the Port Enable (/DS1) (DS2).
It is active when the Processor accesses the Port. /INT should be reset to a high at this time.

CRI PORT

NO INPUT FROM CRI

1. Check the settings of the recorder and refer to the CRI Initialization Procedures in the User Guide.
2. Check the jumpering of the IJA for CRIS.

MIO
Debugging Information

3. Check the CRI Rate Jumpers. Refer to the User Guide.
4. Check to insure that Input Data appears at U25-2. If Data appears, check the operation of the shift registers at U24 and U25. If no Data appears, check the zero crossing detector at U34.

Refer to the CRI Theory of Operation for further timing problems in this area.

5. Check the setting of U19-7 (Read Phase Jumper).

Figure 9

Jumper Settings for Test Programs

Address Selection (II)

External: Jumper 2 address 40H to 43H
Internal: Jumpers 1 and 6

Input Jumper Area (III.1)

Interrupts are not used.
Data input as follows:

Bit 7 - REIA2
Bit 6 - REIA3
Bit 5 - REIA4
Bit 4 - PIOS
Bit 3 - SIOS
Bit 2 - CRIS
Bit 1 - RRDY
Bit 0 - TRDY

Output Jumper Area (III.2)

CRO - DEIA2
CRI - DEIA3
CR2 - DEIA4

Parallel IO Port Input Strobe (V)

PIO1 - No jumper
PIO2 - No jumper

SIO Configuration Jumper Area (IV.)

No jumper

SIO Baud Jumper Area (IV.2)

Jumpered for 1200 Baud

Cassette Recorder Interface

Read and Write Phase VI - as determined by
initial procedure
Bit rate (VI.I) - set for 1500 bits/second

The above configuration provides the user with all the status information required to run a full RS-232-C EIA interface, a cassette recorder and two parallel input/output ports under program control.

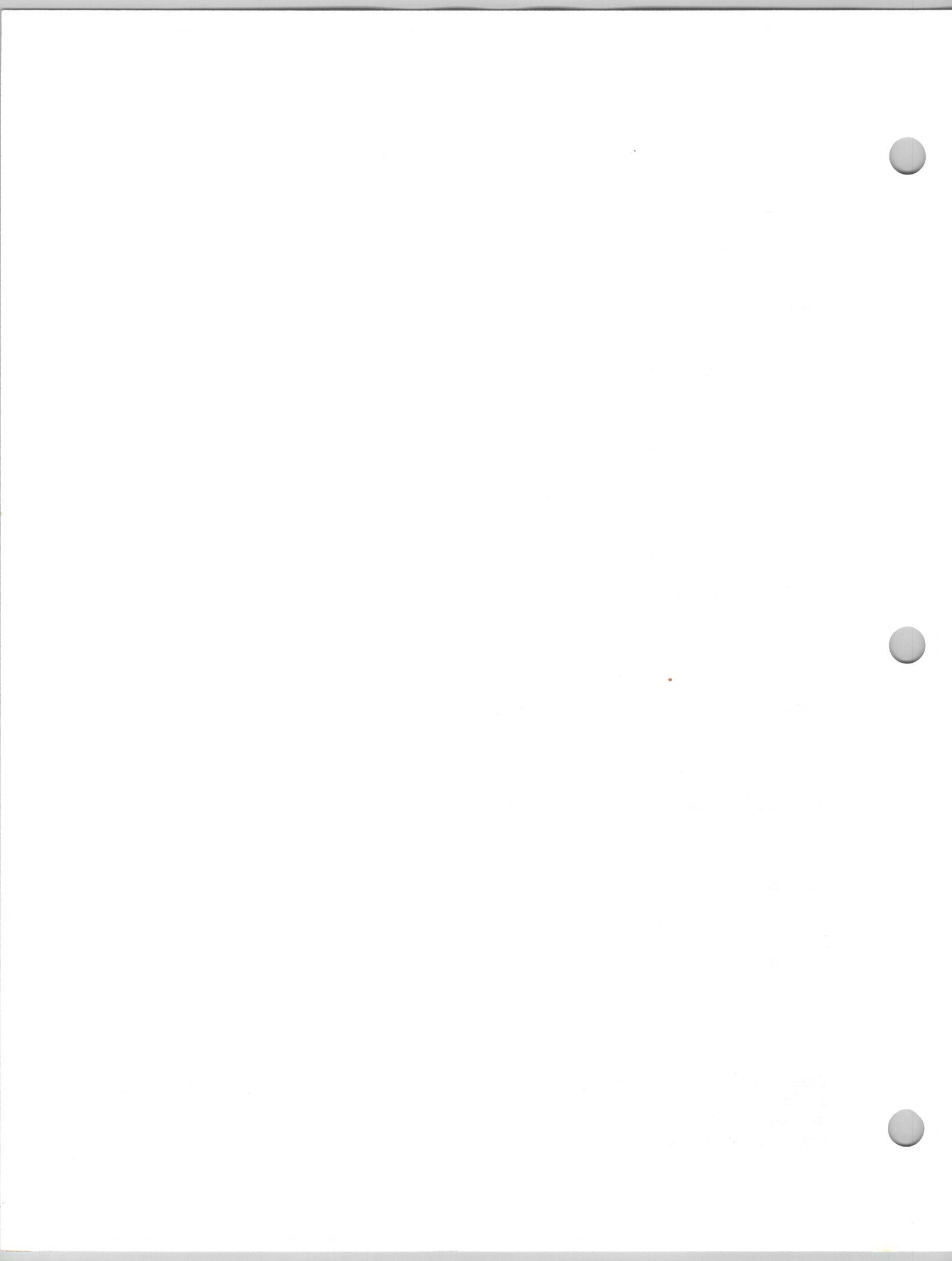
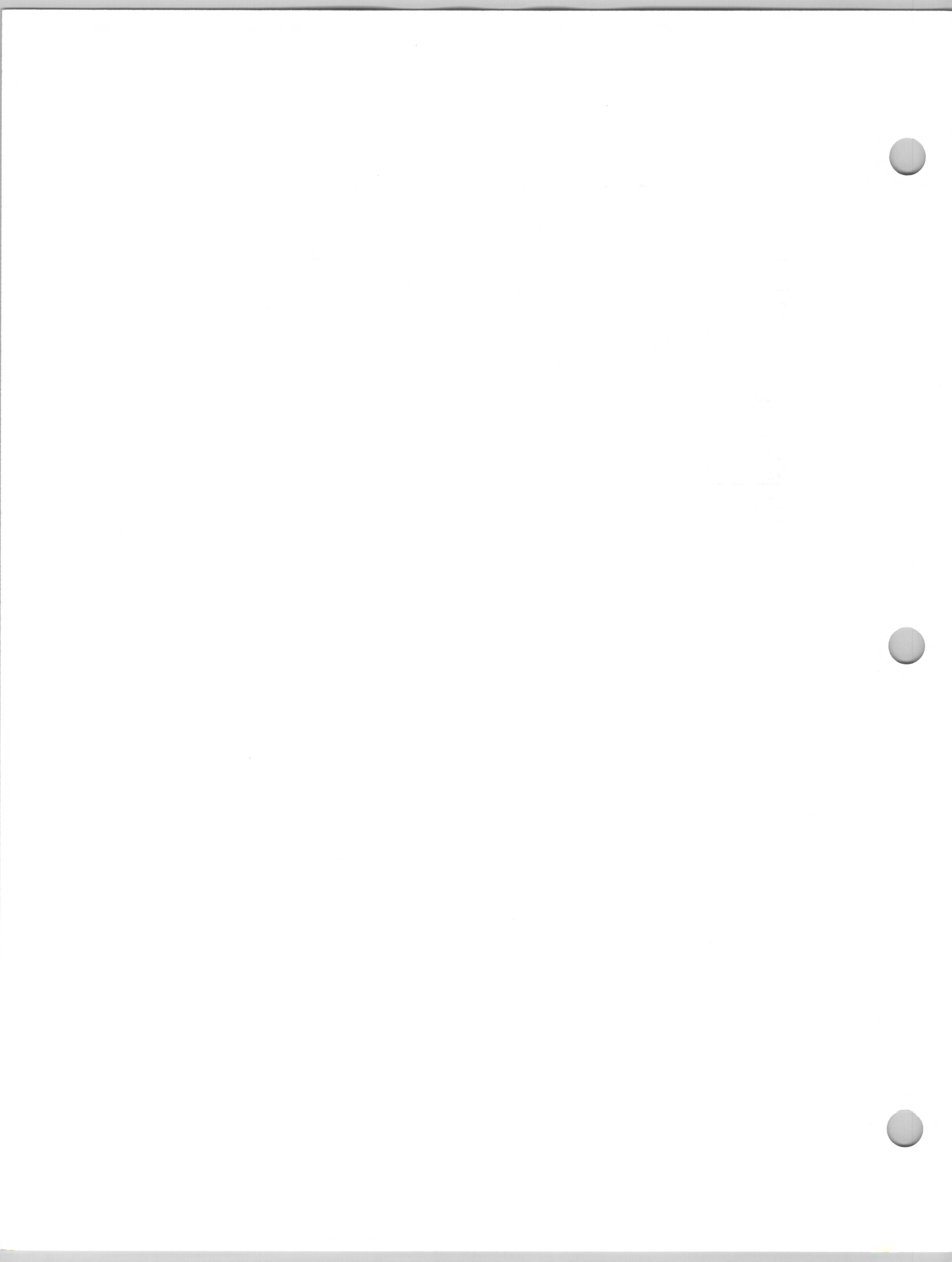


Table 14

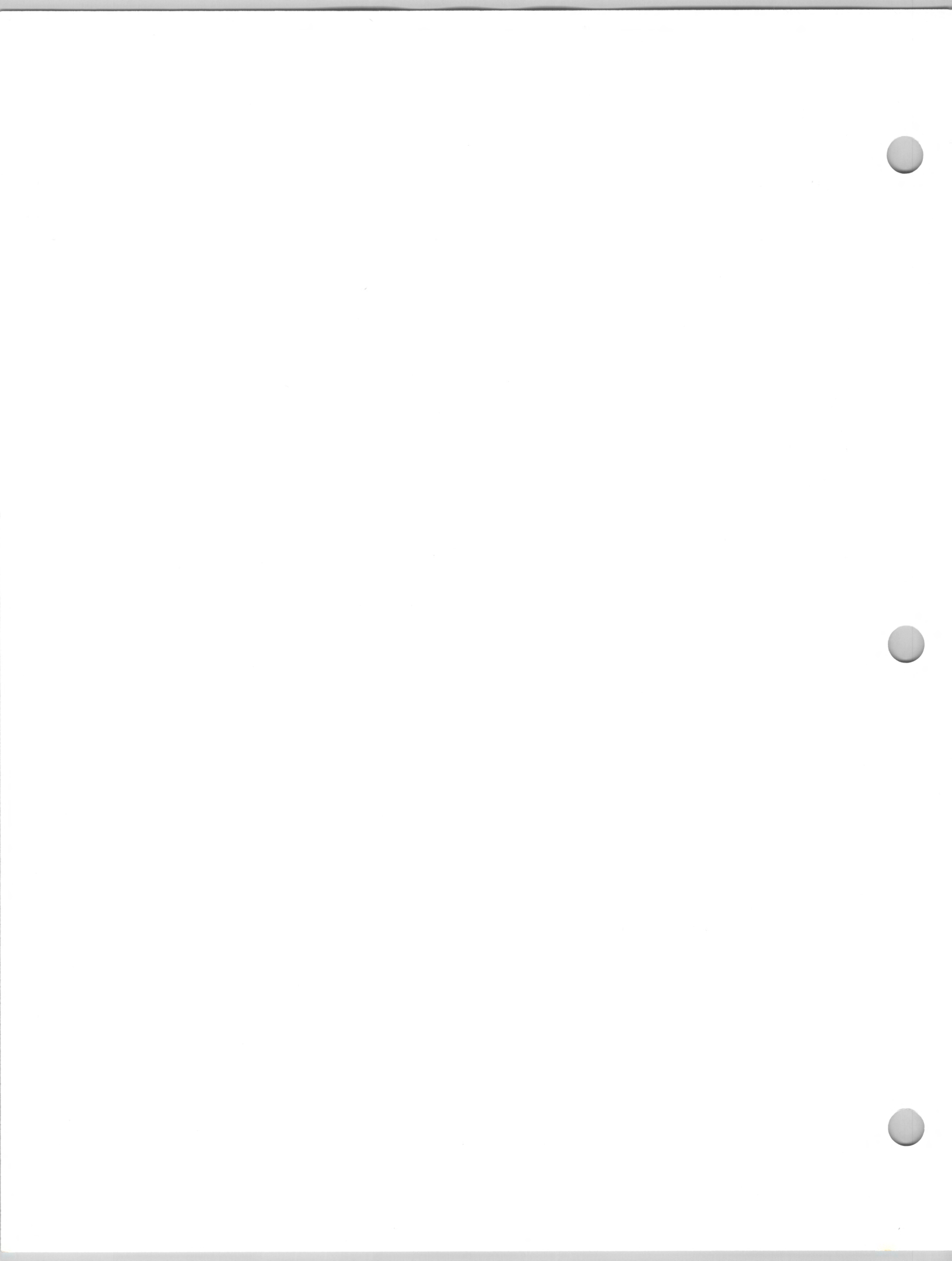
TEST PROGRAM ADDRESSING AND CONTROL

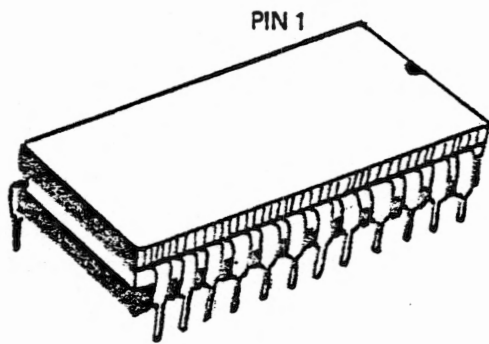
TEST	ENTRY IN HEX	SENSE SWITCHES CONTROL	SENSE LIGHTS DISPLAY
SIO 1	3100	Output Character	Input Character
SIO 2	3103	-----	-----
SIO 3	3106	Transmit Bit Mask	Error Code
PIO 1	3109	Output Character	Output Character
PIO 2	310C	Output Character	Output Character
PIO 3	310F	Output Character	Output Character
CRI Write	3112	-----	Error Code
CRI Read	3115	Sense Light Display	Error Code



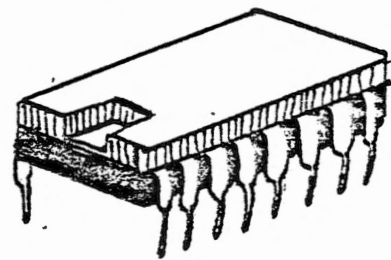
APPENDIX E

COMPONENT ILLUSTRATIONS





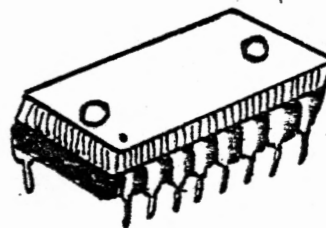
24 PIN I.C. 8212



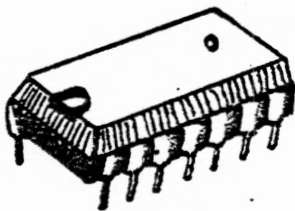
PIN 1

16 PIN I.C.

- 74LS123 (or 74123) 74LS175
- 74LS153 74LS293
- 74LS155 74367
- 74LS163 (or 74LS161) 74LS395
- 8T20



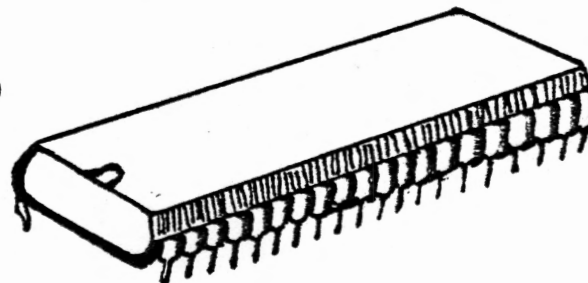
PIN 1



PIN 1

14 PIN I.C.

- | | | |
|--------|--------|----------------------|
| 74LS00 | 74LS32 | 74LS123 (or 74123) |
| 74LS04 | 74LS51 | 74LS153 |
| 74LS05 | 74LS74 | 74LS155 |
| 7406 | 74LS86 | 74LS163 (or 74LS161) |
| 74LS30 | 75188 | |
| 7432 | 75189 | |



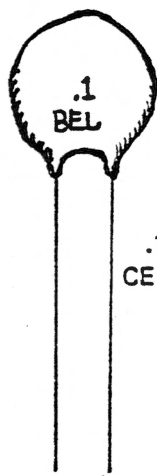
PIN 1

40 PIN

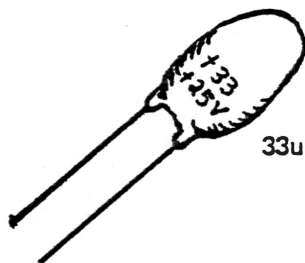
UART

INTEGRATED CIRCUITS/CHIPS

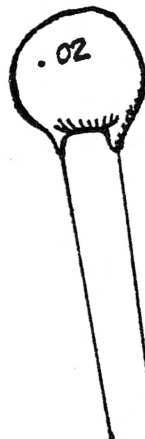
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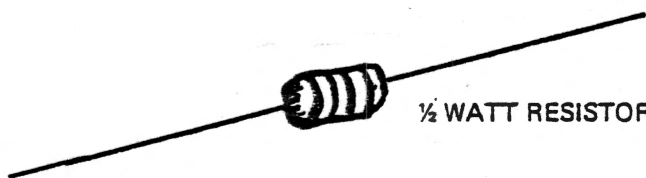
.1 μ F 30V
CERAMIC DISK CAPACITOR



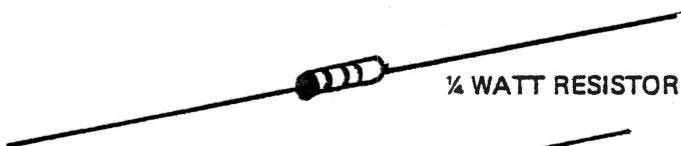
33 μ F 25V TANTALUM CAPACITOR



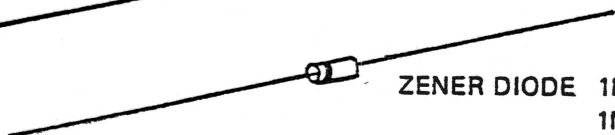
.02 μ F 25V CERAMIC DISK CAPACITOR



1/2 WATT RESISTOR



1/4 WATT RESISTOR

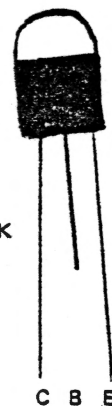


ZENER DIODE 1N4742 (CR1)
1N751A (CR2)

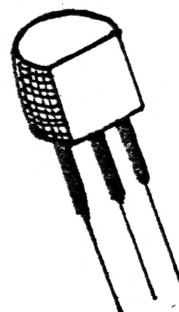


SILICON DIODE 1N914 (CR3)

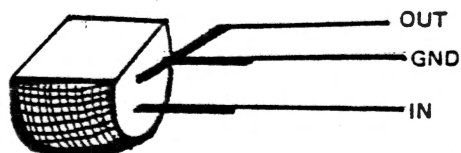
TRANSISTOR 2N3906 (Q1)



CENTER LEAD BENT BACK

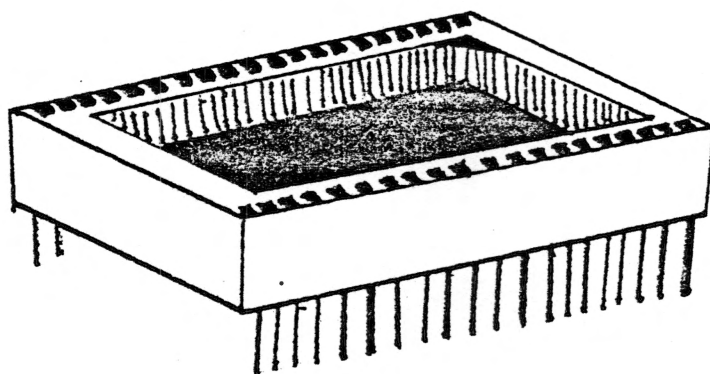


REGULATOR 78L12

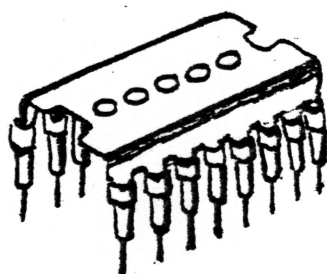


DISCRETE COMPONENTS

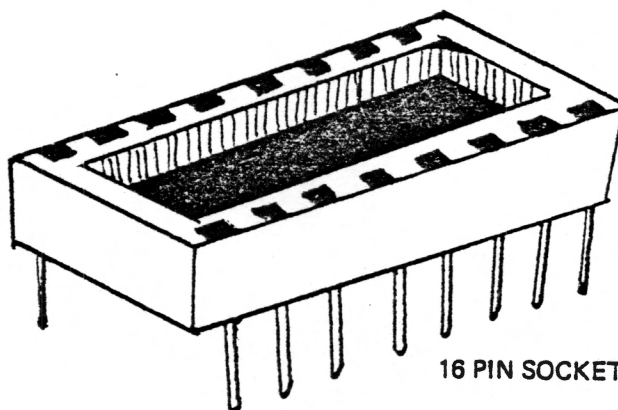
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40 PIN SOCKET



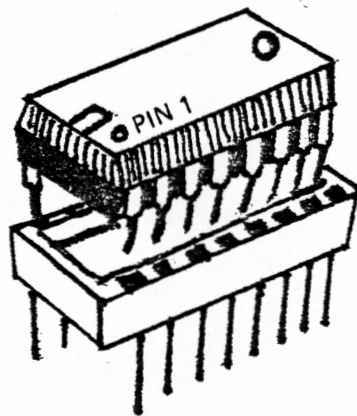
LEAD CARRIER SOCKET



16 PIN SOCKET

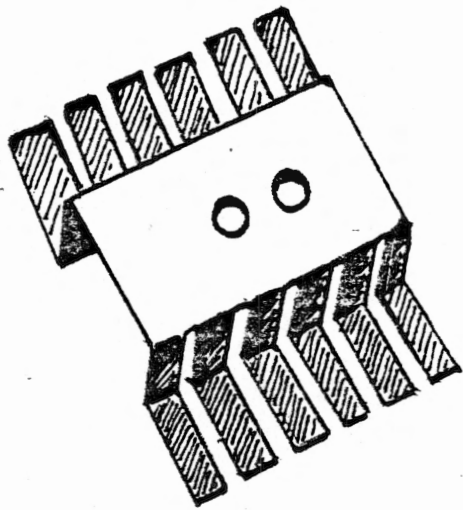
SOCKETS

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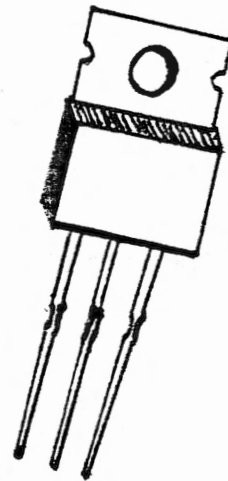


PIN 1

I.C. INSTALLATION
INTO SOCKET



6 PRONG
HEAT SINK



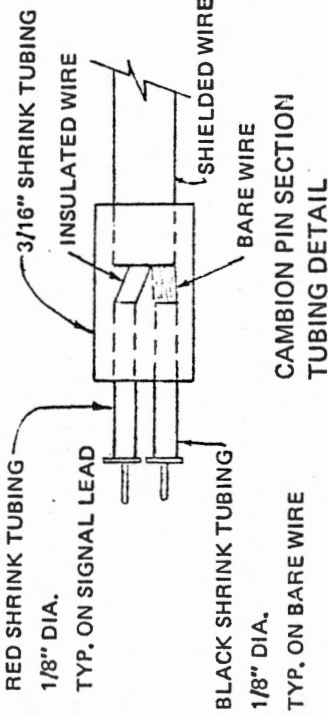
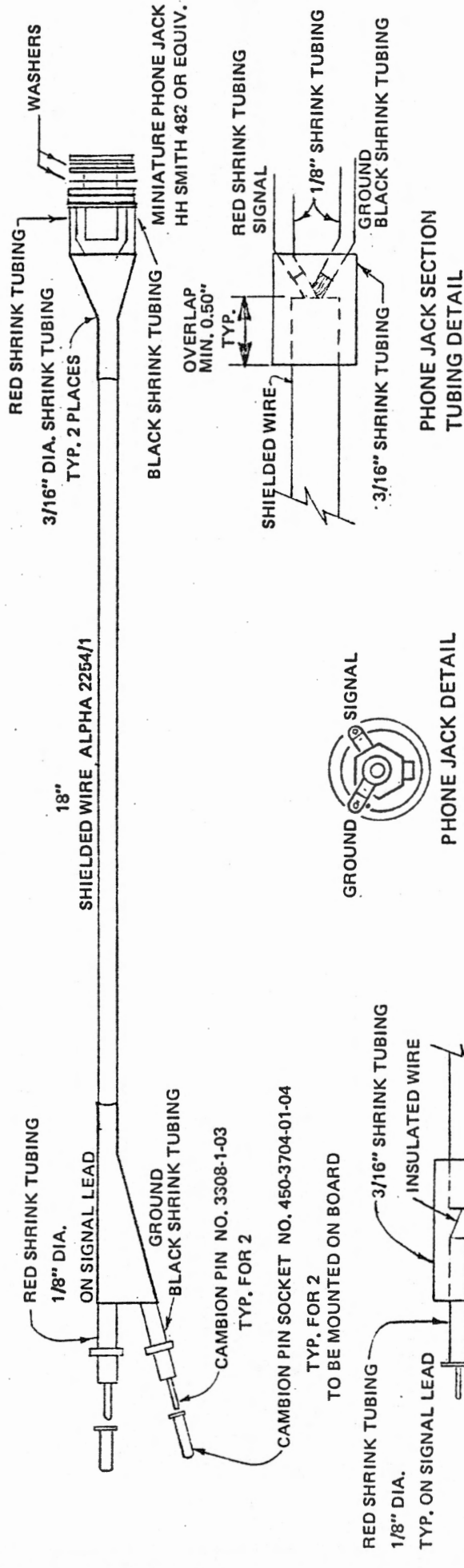
7805 5V POSITIVE VOLTAGE REGULATOR

HEAT SINK & REGULATOR

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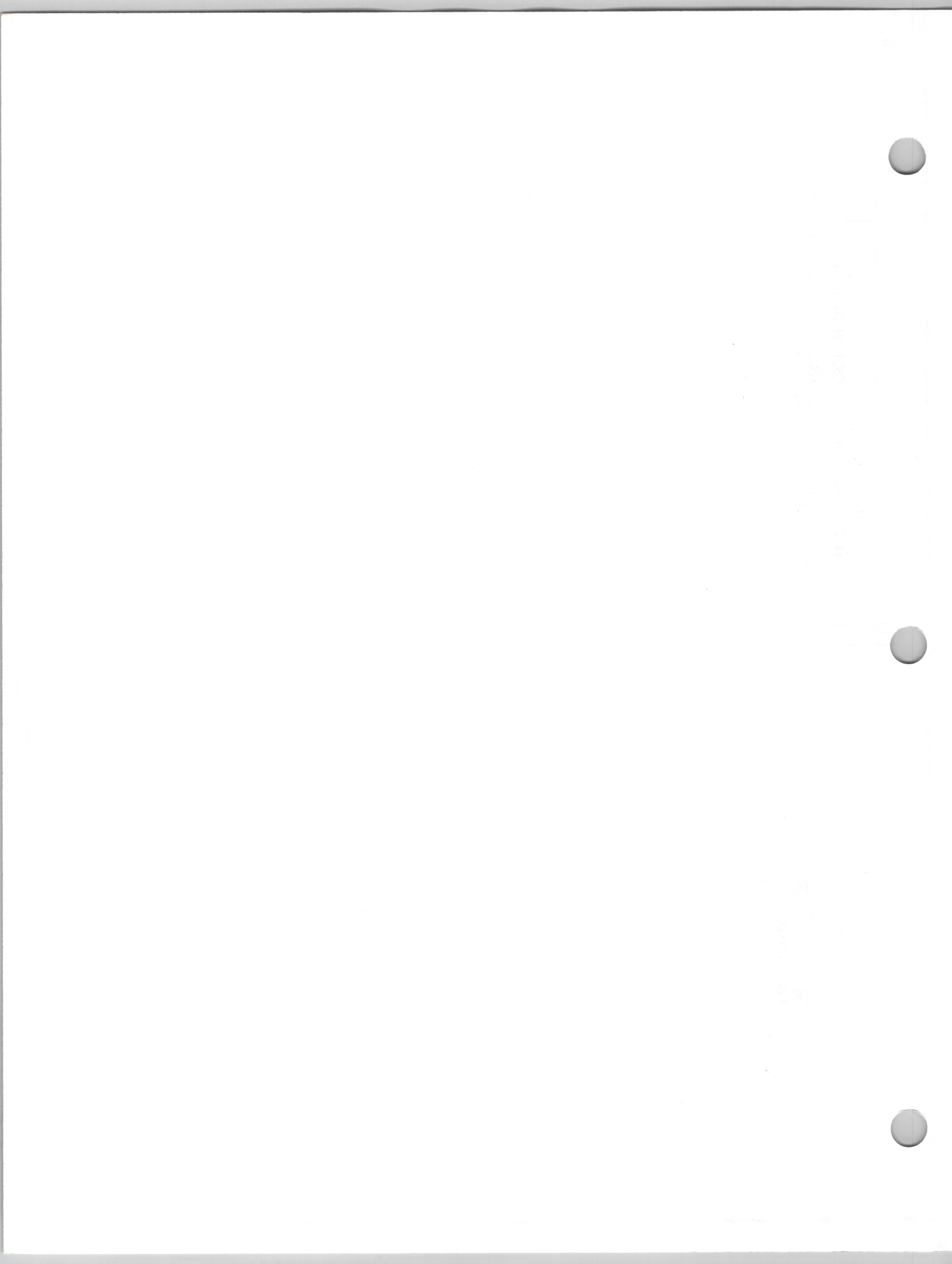
REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL	12/76	ajk
1	MOD. SHRINK TUBING SPECS. ECN 76-0067	12/76	
2	ADDITION JACK DETAIL, MISC. ADDIT'L CALLOUTS FOR CLARIFICATION ECN 77-0007	1/77	MSJ



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APPROVALS	DATE	MIO CABLE M ASSEMBLY	
DRAWN PRU	10/15/76	SCALE	91-0400017
CHECKED J.P.C.	12/6/76	SIZE	DRAWING NO. 91-1040017
A.L.A.	12/7/76	DO NOT SCALE DRAWING	
MADE IN U.S.A.		SHEET 1 OF 1	

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DID YOU FIND ERRORS IN THIS MANUAL? (If so, please specify by page)

IS THE MANUAL UNDERSTANDABLE, USABLE, AND WELL ORGANIZED? (Please make suggestions for improvement)

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PLEASE INDICATE THE TYPE OF USER/READER YOU MOST NEARLY REPRESENT.

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