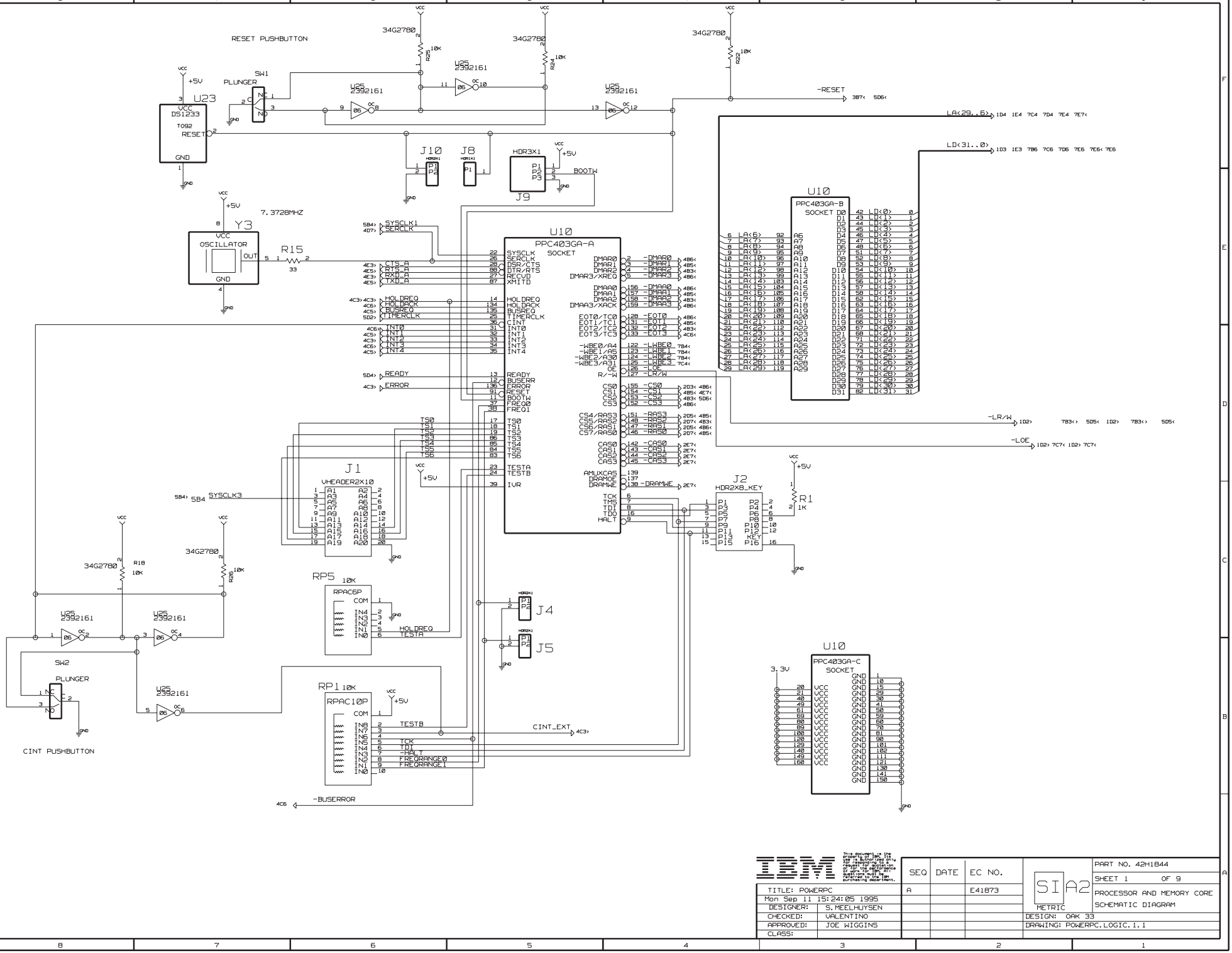
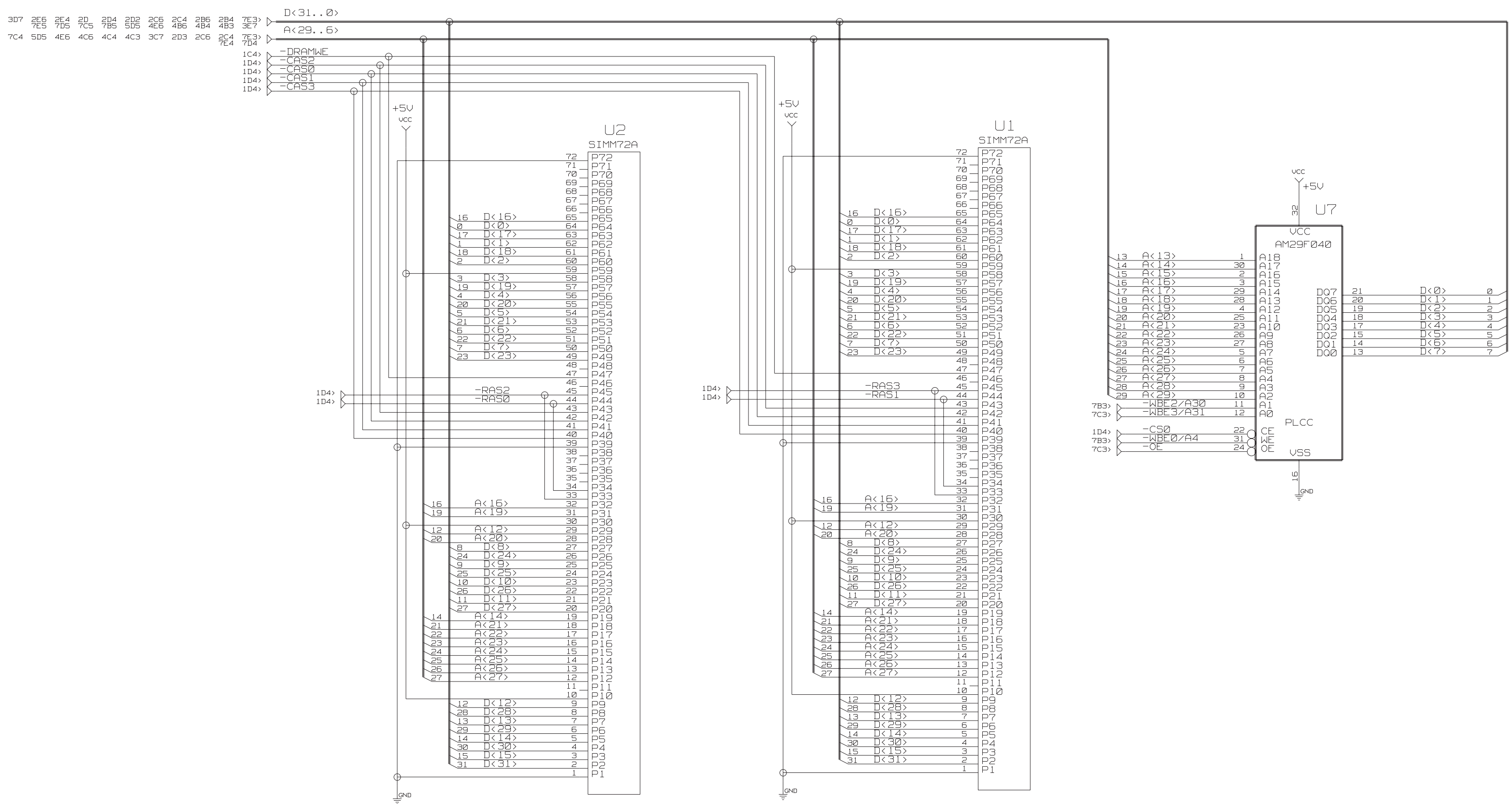


SEQ	DATE	EC NO.
A		E41873

TITLE:	POWERPC
	Mon Sep 11 15:24:05 1995
DESIGNER:	S.MEELHUYSEN
CHECKED:	VALENTINO
APPROVED:	JOE WIGGINS
CLASS:	

SIA2 METRIC

PART NO. 42H1844
SHEET 1 OF 9
PROCESSOR AND MEMORY CORE SCHEMATIC DIAGRAM
DESIGN: OAK 33
DRAWING: POWERPC.LOGIC.1.1



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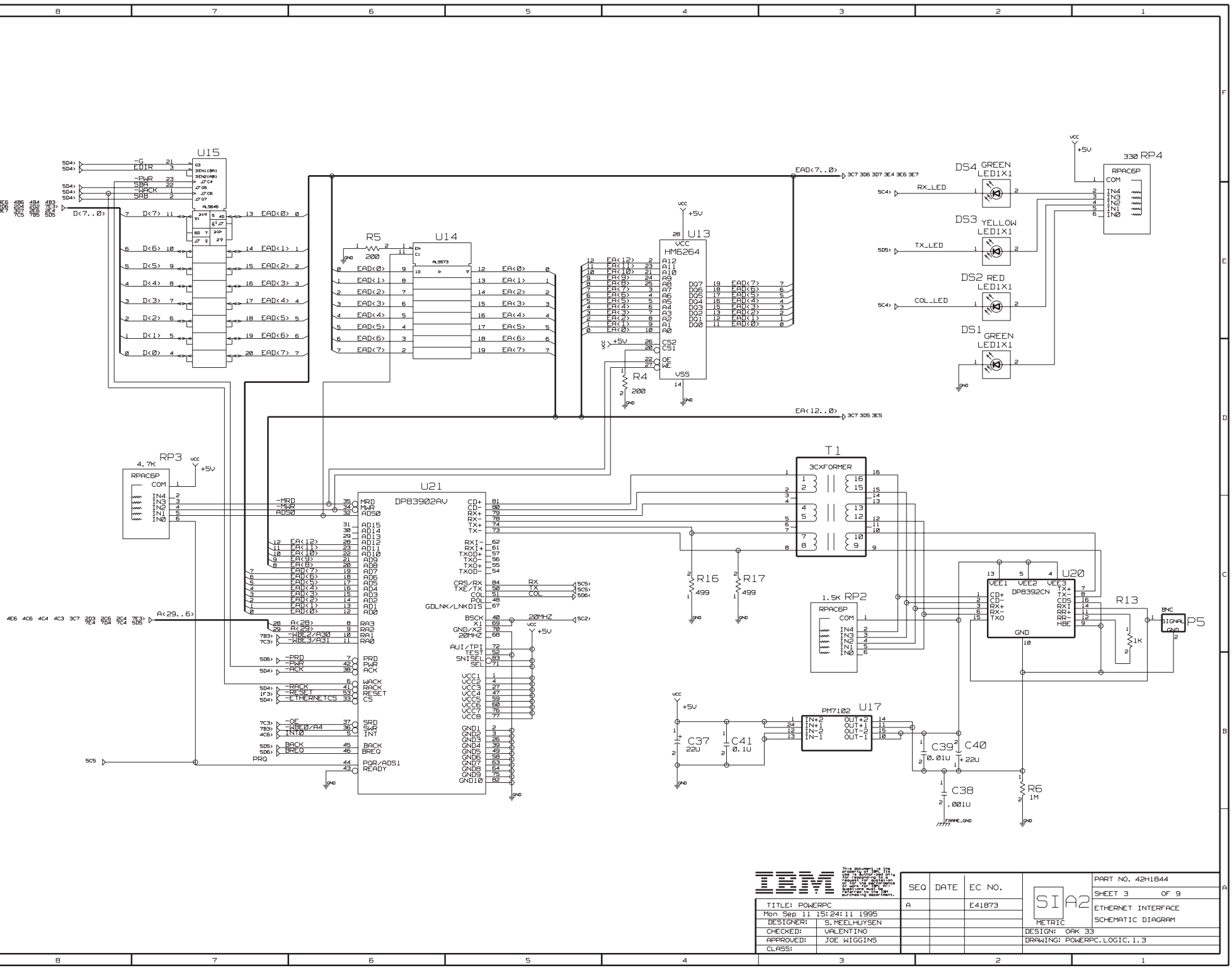
SEQ	DATE	EC NO.
A		E41873

TITLE: POWERPC
Mon Sep 11 15:24:08 1995

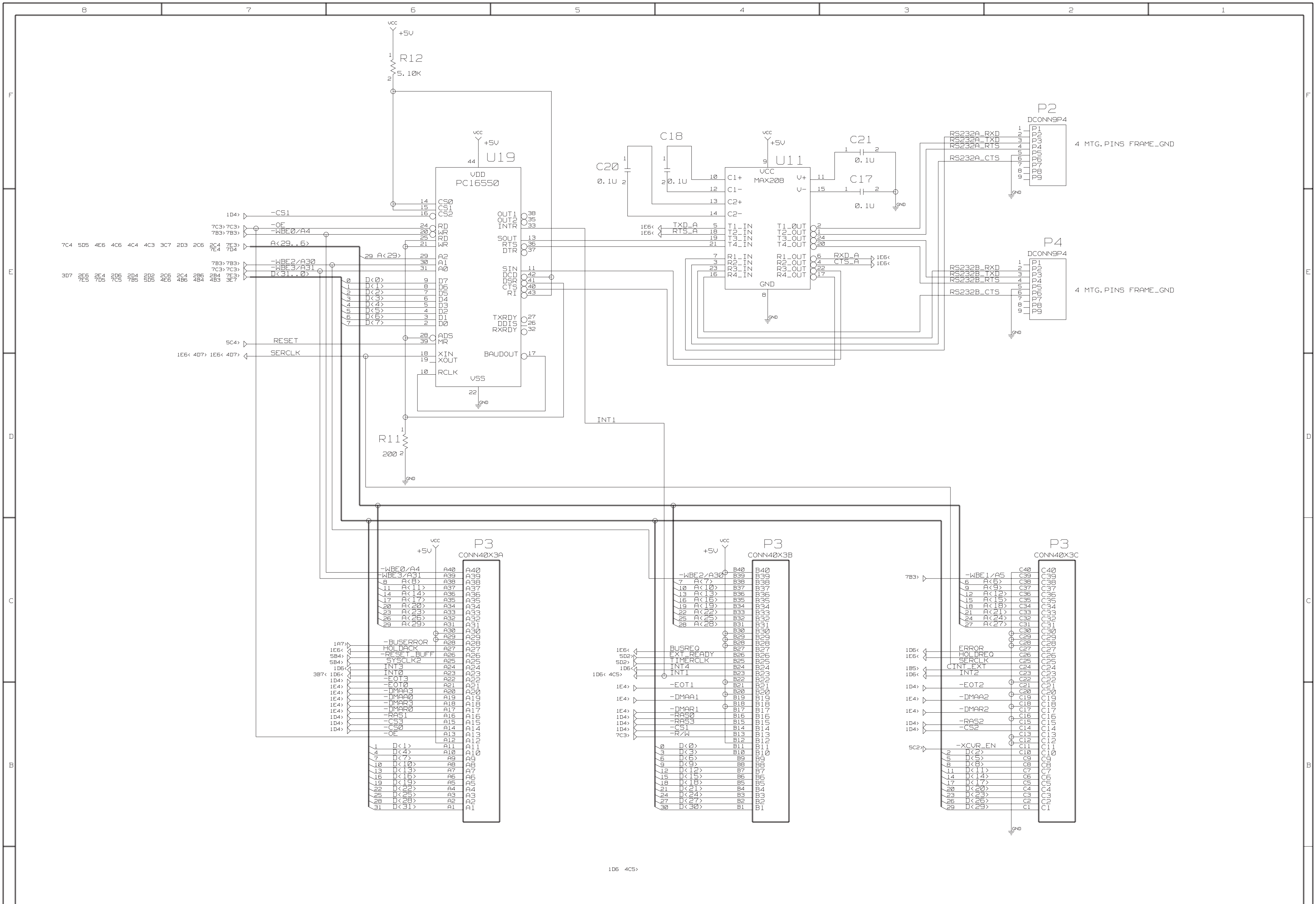
DESIGNER:	S.MEELHUYSEN
CHECKED:	VALENTINO
APPROVED:	JOE WIGGINS
CLASS:	

SI A2 METRIC

PART NO. 42H1844
SHEET 2 OF 9
PROCESSOR AND MEMORY CORE SCHEMATIC DIAGRAM
DESIGN: OAK 33
DRAWING: POWERPC.LOGIC.1.2



TITLE: POWERPC	SEQ	DATE	EC NO.	SIA2 METRIC	PART NO. 42H1844
Mon Sep 11 15:24:11 1995	A		E41873		SHEET 3 OF 9
DESIGNER: S.MEELHUYSEN					ETHERNET INTERFACE
CHECKED: VALENTINO					SCHEMATIC DIAGRAM
APPROVED: JOE WIGGINS				DESIGN: OAK 33	
CLASS:				DRAWING: POWERPC.LOGIC.1.3	


R12
5.10K
R11
200
U19
VDD
PC16550
VSS
U11
VCC
MAX208
GND
C18
C20
C21
C17
0.1U
P2
DCONN9P4
4 MTG.PINS FRAME_GND
P4
DCONN9P4
4 MTG.PINS FRAME_GND
RS232A_RXD
RS232A_TXD
RS232A_RTS
RS232A_CTS
RS232B_RXD
RS232B_TXD
RS232B_RTS
RS232B_CTS
TXD_A
RTS_A
RXD_A
CTS_A
-CS1
-OE
-WBE0/A4
A<29..6>
-WBE2/A30
-WBE3/A31
D<31..0>
RESET
SERCLK
INT1
P3
CONN40X3A
P3
CONN40X3B
P3
CONN40X3C
-BUSERROR
HOLDACK
-RESET_BUFF
SYSCLK2
INT3
INT0
-EOT3
-EOT0
-DMAA3
-DMAA0
-DMAR3
-DMAR0
-RAS1
-CS3
-CS0
BUSREQ
EXT_READY
TIMERCLK
INT4
-EOT1
-DMAA1
-DMAR1
-RAS0
-RAS3
-CS1
-R/W
-WBE1/A5
ERROR
HOLDREQ
SERCLK
CINT_EXT
INT2
-EOT2
-DMAA2
-DMAR2
-RAS2
-CS2
-XCVR_EN
1D6 4C5>

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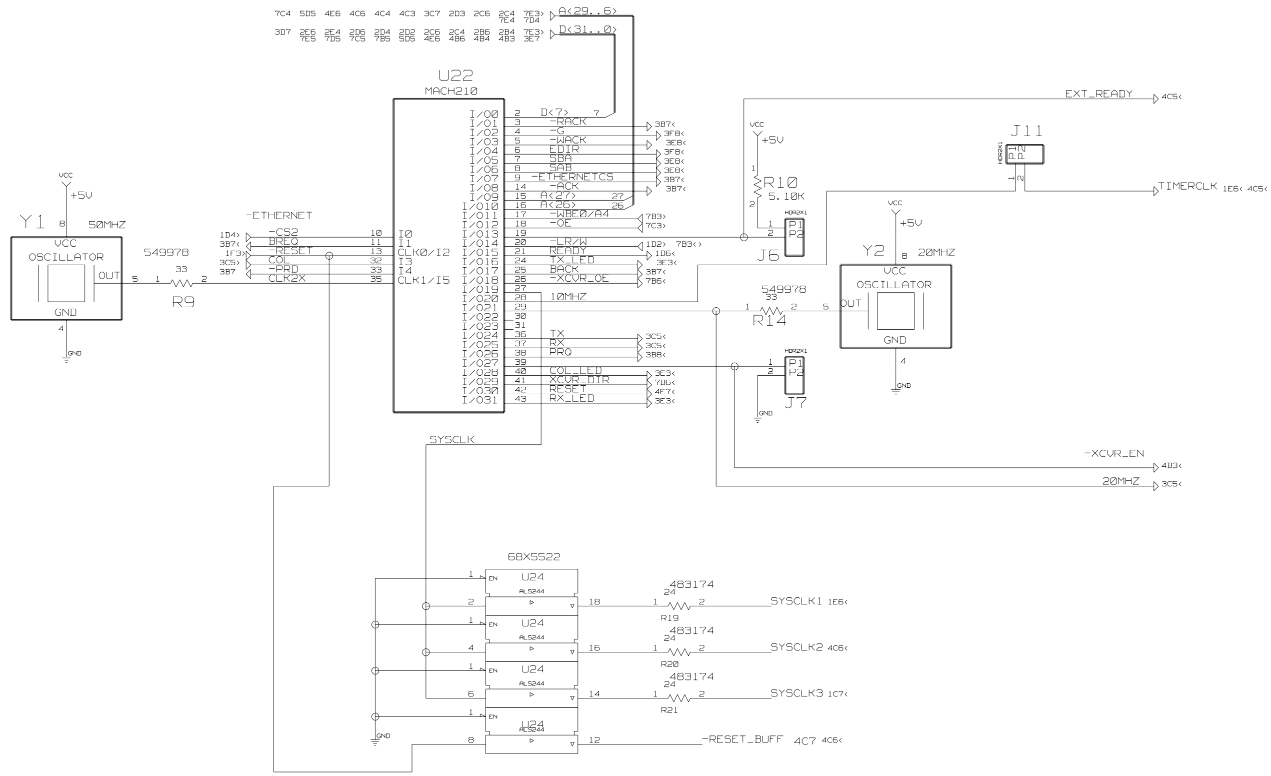
SEQ	DATE	EC NO.
A		E41873

TITLE: POWERPC
Mon Sep 11 15:24:14 1995
DESIGNER: S.MEELHUYSEN
CHECKED: VALENTINO
APPROVED: JOE WIGGINS
CLASS:

SI A2
METRIC

PART NO. 42H1844
SHEET 4 OF 9
SERIAL INTERFACE
SCHEMATIC DIAGRAM
DESIGN: OAK 33
DRAWING: POWERPC.LOGIC.1.4



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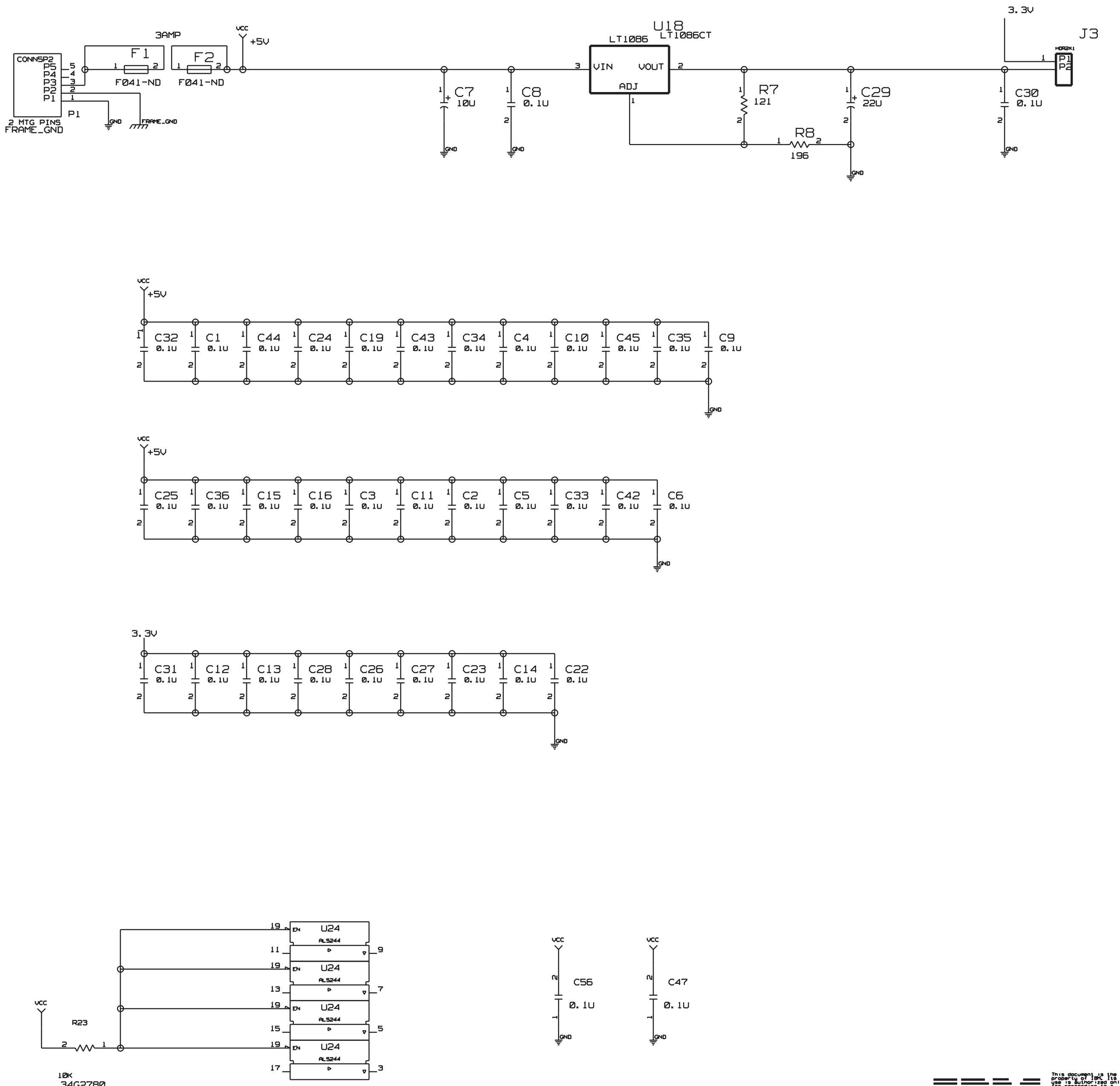
TITLE: POWERPC		
Mon Sep 11 15:24:17 1995		
DESIGNER:	S.MEELHUYSEN	
CHECKED:	VALENTINO	
APPROVED:	JOE WIGGINS	
CLASS:		

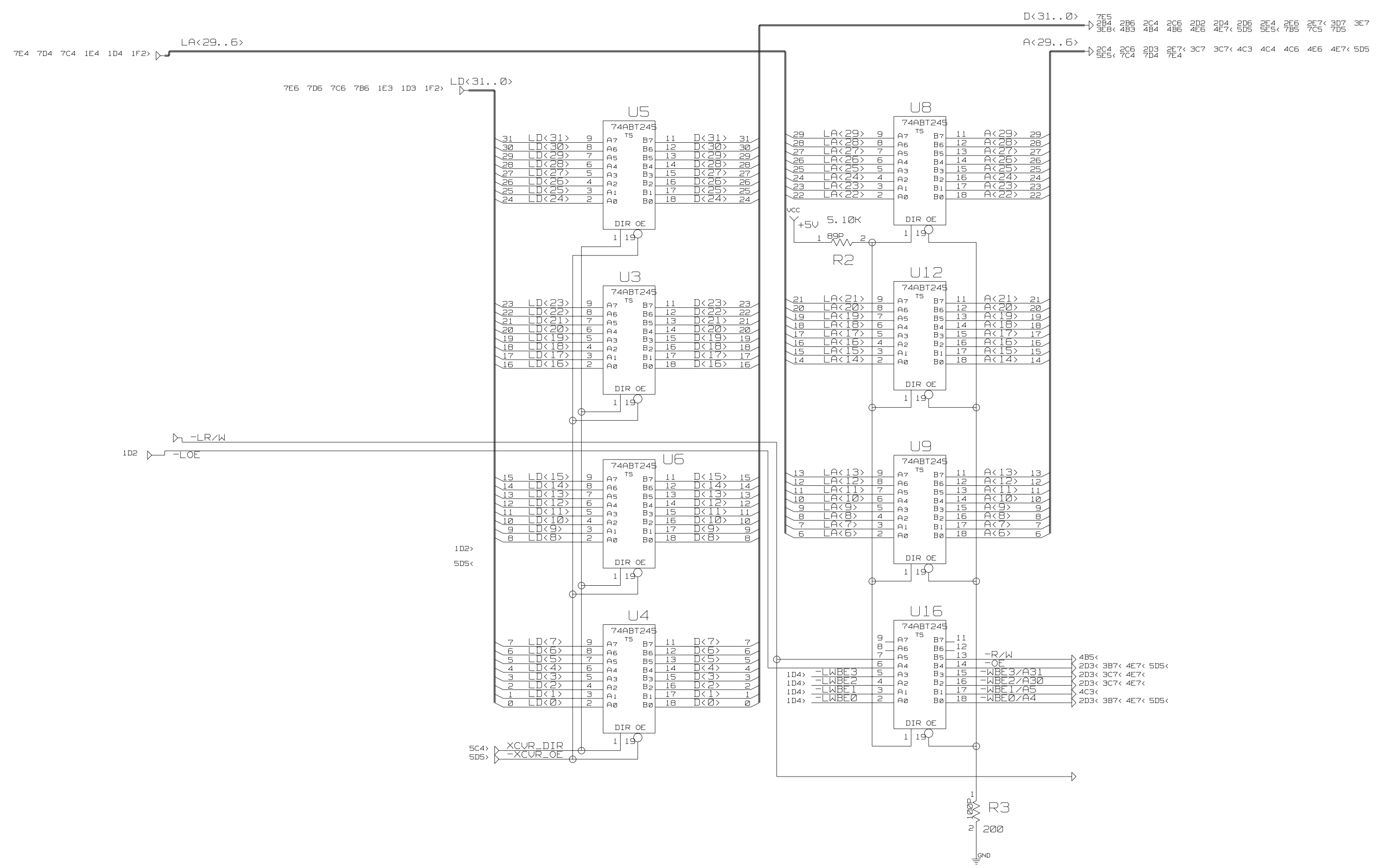
SEQ	DATE	EC NO.
A		E41873

SI A2 METRIC

PART NO. 42H1844
SHEET 5 OF 9
GLUE LOGIC
SCHEMATIC DIAGRAM
DESIGN: OAK 33
DRAWING: POWERPC.LOGIC.1.5



IBM	SEQ	DATE	EC NO.	PART NO. 42H1844
TITLE: POWERPC	A		E41873	SHEET 6 OF 9
Mon Sep 11 15:24:19 1995				POWER AND DECOUPLING SCHEMATIC DIAGRAM
DESIGNER: S.MEELHUYSEN				SIA2 METRIC
CHECKED: VALENTINO				DESIGN: OAK 33
APPROVED: JOE WIGGINS				DRAWING: POWERPC.LOGIC.1.6
CLASS:				



TITLE:	POWERPC
	Mon Sep 11 15:24:23 1995
DESIGNER:	S.MEELHUYSEN
CHECKED:	VALENTINO
APPROVED:	JOE WIGGINS
CLASS:	

SEQ	DATE	EC NO.
A		E41873

SIA2 METRIC

PART NO. 42H1844

SHEET 7 OF 9

PROCESSOR AND MEMORY CORE SCHEMATIC DIAGRAM

DESIGN: OAK 33

DRAWING: POWERPC.LOGIC.1.7

```
       *** Signal Cross-Reference ***
          --- for the entire design --

+5V            1B6 1D3 1D6 1E7 1F5 1F7 2E3 2E5 2E6
              3B4 3C5 3D4 3D7 3E4 3F1 4C4 4C6 4F4
              4F6 5D4 5D7 6D7 6E7 6F7 7D4
-ACK           5D4> 3B7<
-BUSERROR      1A7> 4C6<
-CAS0          1D4> 2E7<
-CAS1          1D4> 2E7<
-CAS2          1D4> 2E7<
-CAS3          1D4> 2E7<
-CS0           1D4> 2D3< 4B6<
-CS1           1D4> 4B5< 4E7<
-CS2           1D4> 4B3< 5D6<
-CS3           1D4> 4B6<
-DMAA0         1E4> 4B6<
-DMAA1         1E4> 4B5<
-DMAA2         1E4> 4B3<
-DMAA3         1E4> 4B6<
-DMAR0         1E4> 4B6<
-DMAR1         1E4> 4B5<
-DMAR2         1E4> 4B3<
-DMAR3         1E4> 4B6<
-DRAMWE        1C4> 2E7<
-EOT0          1E4> 4B6<
-EOT1          1E4> 4B5<
-EOT2          1D4> 4B3<
-EOT3          1D4> 4C6<
-ETHERNETCS    5D4> 3B7<
-G             5D4> 3F8<
-HALT          1B6
-LOE           1D2> 7C7<
-LR/W          1D2> 7B3<> 5D5<
-LWBE0         1D4> 7B4<
-LWBE1         1D4> 7B4<
-LWBE2         1D4> 7B4<
-LWBE3         1D4> 7C4<
-MRD           3C7
-MWR           3C7
-OE            7C3> 2D3< 3B7< 4E7< 5D5<
-PRD           5D6> 3B7<
-PWR           3B7 3E8
-R/W           7C3> 4B5<
-RACK          5D4> 3B7<
-RAS0          1D4> 2D7< 4B5<
-RAS1          1D4> 2D5< 4B6<
-RAS2          1D4> 2D7< 4B3<
-RAS3          1D4> 2D5< 4B5<
-RESET         1F3> 3B7< 5D6<
-RESET_BUFF    5B4> 4C6<
-WACK          5D4> 3E8<
-WBE0/A4       7B3> 2D3< 3B7< 4E7< 5D5<
-WBE1/A5       7B3> 4C3<
-WBE2/A30      7B3> 2D3< 3C7< 4E7<
-WBE3/A31      7C3> 2D3< 3C7< 4E7<
-XCVR_EN       5C2> 4B3<
-XCVR_OE       5D5> 7B6<
3.3V           1B3 6C7 6F3
10MHZ          5D5
20MHZ          5C2> 3C5<
A <29..6>      7E3> 2C4 2C6 2D3 2E7< 3C7 3C7< 4C3
              4C4 4C6 4E6 4E7< 5D5 5E5< 7C4 7D4
              7E4
ADS0           3C7
BACK           5D5> 3B7<
BOOTW          1E5
BREQ           5D6> 3B7<
BUSREQ         4C5> 1E6<
CINT_EXT       1B5> 4C3>
CLK2X          5D6
COL            3C5> 5D6<
COL_LED        5C4> 3E3<
CTS_A          4E3> 1E6<
D <31..0>      7E3> 2B4 2B6 2C4 2C6 2D2 2D4 2D6
              2E4 2E6 2E7< 3D7 3E7 3E8< 4B3 4B4
              4B6 4E6 4E7< 5D5 5E5< 7B5 7C5 7D5
              7E5
EA <12..0>     3D3> 3C7 3D5 3E5
EAD <7..0>     3F3> 3C7 3D6 3D7 3E4 3E6 3E7
EDIR           5D4> 3F8<
ERROR          4C3> 1D6<
EXT_READY      5D2> 4C5<
FREQRANGE0     1B6
FREQRANGE1     1B6
HOLDACK        4C6> 1E6<
HOLDREQ        4C3> 1E6<
INT0           4C6> 1D6< 3B7<
INT1           4C5> 1D6<
INT2           4C3> 1D6<
INT3           4C6> 1D6<
INT4           4C5> 1D6<
LA <29..6>     1F2> 1D4 1E4 7C4 7D4 7E4 7E7<
LD <31..0>     1F2> 1D3 1E3 7B6 7C6 7D6 7E6 7E6<
              7E6
PRQ            5C5> 3B8<
READY          5D4> 1D6<
RESET          5C4> 4E7<
RS232A_CTS     4F3
RS232A_RTS     4F3
RS232A_RXD     4F3
RS232A_TXD     4F3
RS232B_CTS     4E3
RS232B_RTS     4E3
RS232B_RXD     4E3
RS232B_TXD     4E3
RTS_A          4E5> 1E6<
RX             5C5> 3C5
```

```
RXD_A          4E3> 1E6<
RX_LED         5C4> 3E3<
SAB            5D4> 3E8<
SBA            5D4> 3E8<
SERCLK         4D7> 1E6<
SYSCLK         5C5
SYSCLK1        5B4> 1E6<
SYSCLK2        5B4> 4C6<
SYSCLK3        5B4> 1C7<
TCK            1B6
TDI            1B6
TESTA          1C6
TESTB          1B6
TIMERCLK       5D2> 1E6< 4C5<
TS0            1D6
TS1            1D6
TS2            1D6
TS3            1D6
TS4            1D6
TS5            1D6
TS6            1D6
TX             5C5> 3C5<
TXD_A          4E5> 1E6<
TX_LED         5D5> 3E3<
XCVR_DIR       5C4> 7B6<
```

IBM

	SEQ	DATE	EC NO.		
TITLE: NO TITLE	A		E41873	SI A2 METRIC	PART NO. 42H1844
Mon Sep 11 15:24:03 1995					SHEET 8 OF 9
DESIGNER:					CROSS REFERENCE
CHECKED:				DESIGN: OAK 33	
APPROVED:				DRAWING: CREFOUT.LOGIC.1.8	
CLASS:					

*** Unit Cross-Reference ***

--- for the entire design --

C1	CAPACITOR	6E7
C2	CAPACITOR	6D6
C3	CAPACITOR	6D6
C4	CAPACITOR	6E6
C5	CAPACITOR	6D6
C6	CAPACITOR	6D5
C7	CAPACITOR	6F6
C8	CAPACITOR	6F5
C9	CAPACITOR	6E5
C10	CAPACITOR	6E5
C11	CAPACITOR	6D6
C12	CAPACITOR	6C7
C13	CAPACITOR	6C7
C14	CAPACITOR	6C6
C15	CAPACITOR	6D7
C16	CAPACITOR	6D6
C17	CAPACITOR	4F3
C18	CAPACITOR	4F5
C19	CAPACITOR	6E6
C20	CAPACITOR	4F5
C21	CAPACITOR	4F3
C22	CAPACITOR	6C5
C23	CAPACITOR	6C6
C24	CAPACITOR	6E6
C25	CAPACITOR	6D7
C26	CAPACITOR	6C6
C27	CAPACITOR	6C6
C28	CAPACITOR	6C6
C29	CAPACITOR	6F4
C30	CAPACITOR	6F3
C31	CAPACITOR	6C7
C32	CAPACITOR	6E7
C33	CAPACITOR	6D5
C34	CAPACITOR	6E6
C35	CAPACITOR	6E5
C36	CAPACITOR	6D7
C37	CAPACITOR	3B4
C38	CAPACITOR	3B2
C39	CAPACITOR	3B2
C40	CAPACITOR	3B2
C41	CAPACITOR	3B4
C42	CAPACITOR	6D5
C43	CAPACITOR	6E6
C44	CAPACITOR	6E7
C45	CAPACITOR	6E5
C47	CAPACITOR	6B5
C56	CAPACITOR	6B5
DS1	LED1X1	3E2
DS2	LED1X1	3E2
DS3	LED1X1	3E2
DS4	LED1X1	3F2
F1	FUSE	6F7
F2	FUSE	6F7
J1	VHEADER2X10	1D6
J2	HDR2X8KEY	1C4
J3	HDR2X1	6F3
J4	HDR2X1	1C5
J5	HDR2X1	1B5
J6	HDR2X1	5D4
J7	HDR2X1	5C4
J8	HDR1X1	1F5
J9	HDR3X1	1E5
J10	HDR2X1	1F6
J11	HDR2X1	5D3
P1	CONN5P2	6F8
P2	DCONN9P4	4F2
P3	CONN40X3	4C2 4C4 4C6
P4	DCONN9P4	4E2
P5	BNC6	3C1
R1	RESISTOR	1C3
R2	RESISTOR	7D4
R3	RESISTOR	7B3
R4	RESISTOR	3D4
R5	RESISTOR	3E6
R6	RESISTOR	3B2
R7	RESISTOR	6F4
R8	RESISTOR	6E4
R9	RESISTOR	5D6
R10	RESISTOR	5D4
R11	RESISTOR	4D6
R12	RESISTOR	4F6
R13	RESISTOR	3C1
R14	RESISTOR	5C4
R15	RESISTOR	1E7
R16	RESISTOR	3C4
R17	RESISTOR	3C4
R18	RESISTOR	1C8
R19	RESISTOR	5B4
R20	RESISTOR	5B4
R21	RESISTOR	5B4
R22	RESISTOR	1F4
R23	RESISTOR	6A8
R24	RESISTOR	1F5
R25	RESISTOR	1F6
R26	RESISTOR	1C7
RP1	RPAC10P	1B6
RP2	RPAC6P	3C3
RP3	RPAC6P	3D7
RP4	RPAC6P	3F1
RP5	RPAC6P	1C6
SW1	PLUNGER	1F7
SW2	PLUNGER	1B8
T1	3CXFORMER	3D3
U1	SIMM72A	2E4
U2	SIMM72A	2E
U3	74ABT245	7D5
U4	74ABT245	7C5
U5	74ABT245	7E5
U6	74ABT245	7C5
U7	AM29F040P	2E3
U8	74ABT245	7E4
U9	74ABT245	7C4
U10	PPC403GA	1B3 1E3 1E5
U11	MAX208	4F4
U12	74ABT245	7D4
U13	HM6264	3E4
U14	ALS573	3E6
U15	ALS646	3F7
U16	74ABT245	7C4
U17	PM7102	3B3
U18	LT1086	6F5
U19	PC16550	4F6
U20	DP8392CN	3C2
U21	DP83902AV	3D6
U22	MACH210	5D5
U23	DS1233	1F7
U24	ALS244	5B5 6A6 6B6
U25	06	1B7 1C7 1C8 1F5 1F5 1F6
Y1	OSCHALFDIPA	5D7
Y2	OSCHALFDIPA	5D4
Y3	OSCHALFDIPA	1E7

IBM

SEQ	DATE	EC NO.
A		E41873

TITLE: NO TITLE
Mon Sep 11 15:24:03 1995
DESIGNER:
CHECKED:
APPROVED:
CLASS:

SI A2
METRIC

PART NO. 42H1844
SHEET 9 OF 9
CROSS REFERENCE
DESIGN: OAK 33
DRAWING: CREFOUT.LOGIC.1.9