PowerPC™

IBM

PowerPC® 405CR Embedded Processor

Up-to-375MIPS integrated device for cost-conscious embedded applications

Highlights

Offers high performance and value for a wide variety of embedded applications, including wired communications, data storage, and pervasive computing devices

Application code compatible with all other PowerPC processors

Built with reusable core-based design principles, so many functions pre-verified in silicon

Utilizes 64-bit CoreConnect™ bus architecture at up to 133MHz, providing high-speed on-chip performance with low latencies

Offers an effective functional and performance upgrade to designs based on PowerPC 403GCX embedded processor

Implements innovative CodePack™ code compression, improving instruction code density and reducing overall system cost

Low power consumption for thermally sensitive environments

PowerPC 405B3 Embedded Core

- 200 or 266MHz CPU core
- Memory Management Unit
- 16KB instruction and 8KB data caches
- Multiply-Accumulate (MAC) function, including fast multiply unit
- 5-stage pipeline
- Timers
- JTAG and non-invasive trace debug logic

SDRAM Controller

- 4 chip selects, 4MB to 256MB per bank
- PC100 (200MHz) and PC133 (266MHz) compliant
- Supports dual- and quad-bank SDRAMs with 11x8 to 13x11 addressing
- Programmable address mapping and timing
- Separate 32-byte read and 128-byte write buffers
- Power management (self-refresh)
- 32-bit external data bus width
- ECC option

External Peripheral Controller

- Supports ROM, EPROM, SRAM, Flash and slave peripheral I/O devices
- 8 banks
- Burst and non-burst devices
- 8-, 16-, 32-bit external data bus width
- Latch data on ready, synchronous or asynchronous
- Parity option
- Programmable address mapping

CodePack Decompression

- Instructions stored in memory in compressed format
- Improves code density up to 40%
- No loss in instruction set capability

External Bus Master Controller

- Allows external masters to access SDRAM

DMA Controller

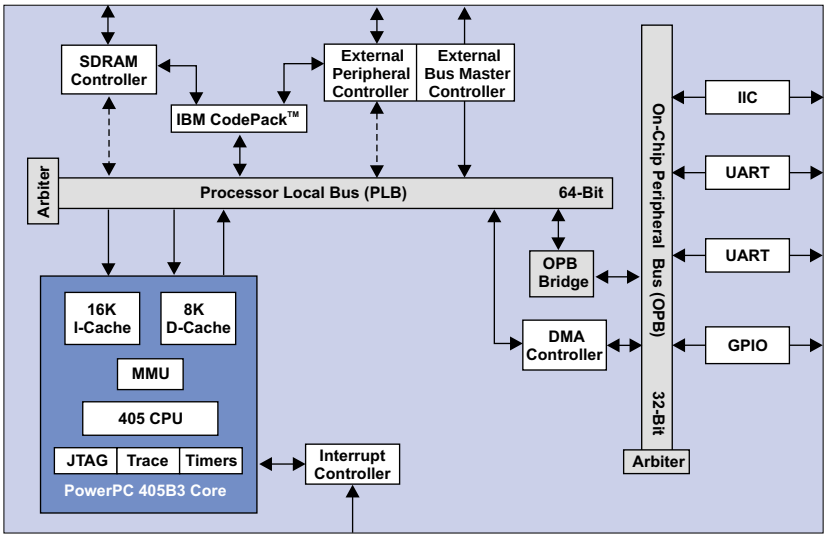
- 4 independent channels
- 8-, 16-, 32-bit peripheral support
- Supports buffered memory-to-peripheral, peripheral-to-memory and memory-to-memory transfers
- Scatter/gather capability with command/data chaining
- 32-byte data buffer
- Supports transfers between SDRAM, PCI, internal UARTs, and devices on the external peripheral bus

Other On-Chip Peripherals

- 2 serial ports (16550), 9-pin and 4-pin
- Master and slave IIC controller, compliant with Phillips I^2C spec
- Up to 23 general purpose I/Os
- Interrupt controller including up to 12 external interrupts

PowerPC 405CR embedded processor in 27mm x 27mm, Enhanced PBGA package

PowerPC 405CR Specifications	
Technology	0.25µm (0.18µm L_{eff}) CMOS SA-12E
Performance (est.)	282 Dhrystone 2.1 MIPS @ 200MHz 375 Dhrystone 2.1 MIPS @ 266Hz
Frequency (CPU / SDRAM/ EBC)	200/100/50 MHz 266/133/66 MHz
Typical Power Dissipation (est.)	0.8W
Signal I/Os	223
Case Temperature Range	-40° C to 85° C
Power Supply	2.5V (logic), 3.3V (I/O), supports 5V I/Os
Packaging	316-Ball, Enhanced PBGA (27mm x 27mm)



PowerPC 405CR block diagram

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