PowerPC™

IBM

PowerPC® 405GP Embedded Processor

Highly integrated, up-to-375MIPS device for networked applications

Highlights

Offers high performance and rich peripheral mix for networked applications, including wired communications, data storage, and pervasive computing devices

Extends the scalability of the PowerPC processor family

Application code compatible with all other PowerPC processors

Utilizes 64-bit CoreConnect™ bus architecture at up to 133MHz, providing high performance on-chip with low latencies

Implements innovative CodePack™ code compression, significantly improving instruction code density and reducing overall system cost

On-chip SRAM holds critical code and data, and provides single cycle access

Provides small form-factor package options for integration into dense applications

Low power consumption for thermally sensitive environments

As a Blue Logic™ superstructure, provides a foundation for custom derivative designs of the 405GP to be done quickly and easily

PowerPC 405B3 Embedded Core

- 200 or 266MHz 32-bit RISC CPU core
- Memory Management Unit
- 16KB instruction and 8KB data caches
- Multiply-Accumulate (MAC) function, including fast multiply unit
- 5-stage pipeline
- Timers
- JTAG and non-invasive trace debug logic
- 4KB single cycle SRAM

SDRAM Controller

- 4 chip selects, 4MB to 256MB per bank
- PC100 (200MHz) and PC133 (266MHz) compliant
- Supports dual- and quad-bank SDRAMs with 11x8 to 13x11 addressing
- Programmable address mapping and timing
- Separate 32-byte read and 128-byte write buffers
- Power management (self-refresh)
- 32-bit external data bus width
- ECC option

External Peripheral Controller

- Supports ROM, EPROM, SRAM, Flash and slave peripheral I/O devices
- 8 banks
- Burst and non-burst devices
- 8-, 16-, 32-bit external data bus width
- Latch data on ready, synchronous or asynchronous
- Parity option
- Programmable address mapping

External Bus Master Controller

- Allows external masters to access SDRAM and PCI

DMA Controller

- 4 independent channels
- 8-, 16-, 32-bit peripheral support

The 405GP offers multiple package options

PowerPC 405GP Specifications	
Technology	0.25µm (0.18µm L_{eff}) CMOS SA-12E
Performance (est.)	282 Dhrystone 2.1 MIPS @ 200MHz 375 Dhrystone 2.1 MIPS @ 266MHz
Frequency (CPU / SDRAM / PCI / EBC)	200/100/66/50 MHz 266/133/66/66 MHz
Number of Transistors (est.)	4.8 million
Typical Power Dissipation (est.)	1.1W
Signal I/Os	300
Case Temperature Range	-40° C to 85° C
Power Supply	2.5V (logic), 3.3V (I/O), supports 5V I/Os
Packaging	456-Ball, Enhanced PBGA (35mm x 35mm) 456-Ball, Enhanced PBGA (27mm x 27mm) 413-Ball, Enhanced PBGA (25mm x 25mm)

- Supports buffered memory-to-peripheral, peripheral-to-memory and memory-to-memory transfers
- Scatter/gather capability with command/data chaining
- 32-byte data buffer
- Supports transfers between SDRAM, PCI, internal UARTs, and devices on the external peripheral bus

PCI Interface

- 32-bit, PCI V2.2 compatible
- Synchronous operation at 1:1, 1:2, 1:3, and 1:4 of PLB frequency
- Asynchronous operation from 1/8 PLB frequency up to 66MHz maximum
- Read prefetch and posted write buffers from both PCI and PLB sides
- Internal PCI arbiter, supports six PCI masters
- Supports external arbitration
- Optional system boot from PCI

On-Chip Ethernet Support

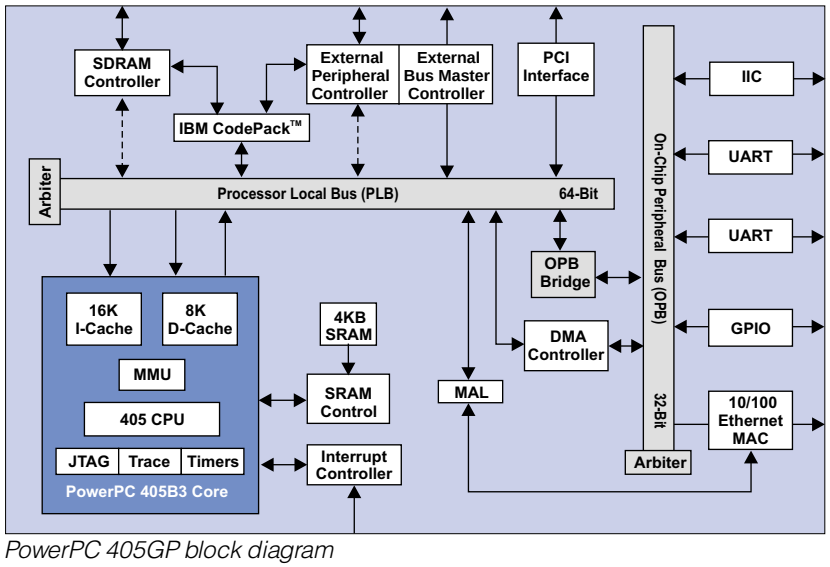
- 10/100 MAC with 2KB Tx and 4KB Rx FIFOs
- Medium Independent Interface (MII) to external physical layer PHY
- Dedicated DMA controller

CodePack Decompression

- Instructions stored in memory in compressed format
- Improves code density up to 40%
- No loss in instruction set capability

Other On-Chip Peripherals

- 2 serial ports (16550), 9-pin and 4-pin
- Master and slave IIC controller, compliant with Phillips I²C spec
- Up to 23 general purpose I/Os
- Interrupt controller including up to 12 external interrupts



PowerPC 405GP block diagram

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