PowerPC™ 440GP Embedded Processor:
High performance SOC for networked applications

IBM® Microelectronics

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Design Objectives and Strategy

- **Develop high performance, highly integrated system on a chip, while utilizing ASIC methodology**
- **Provide a base set of state-of-the-art reusable core IP for future PowerPC 440-based designs**
- **Target integrated features to networked applications**
  - Network infrastructure, network access devices, storage area networks, RAID controllers, et al
- **Maintain aggressive price and power characteristics traditional to PowerPC designs**
- **Provide PowerPC Book E architecture compliance**

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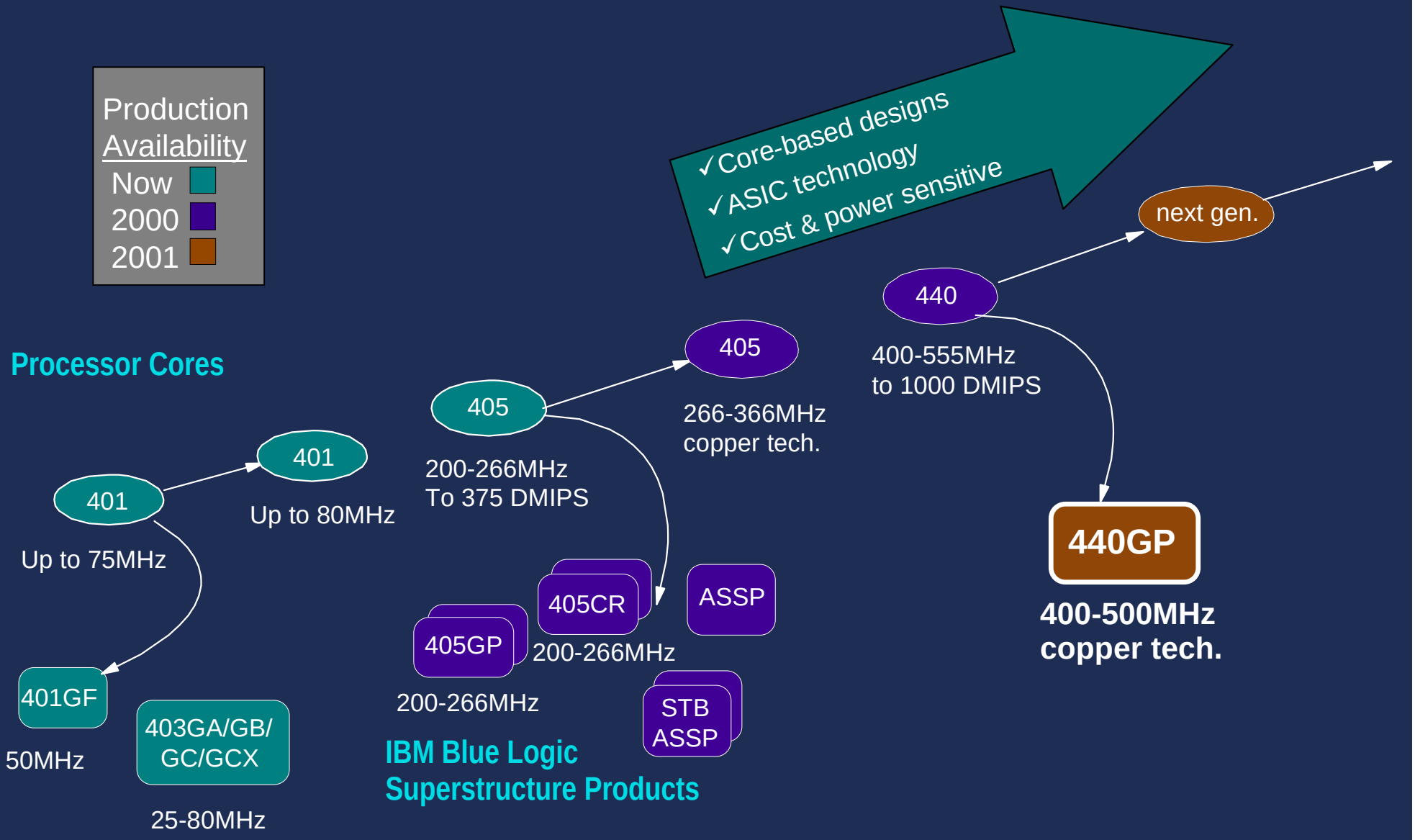
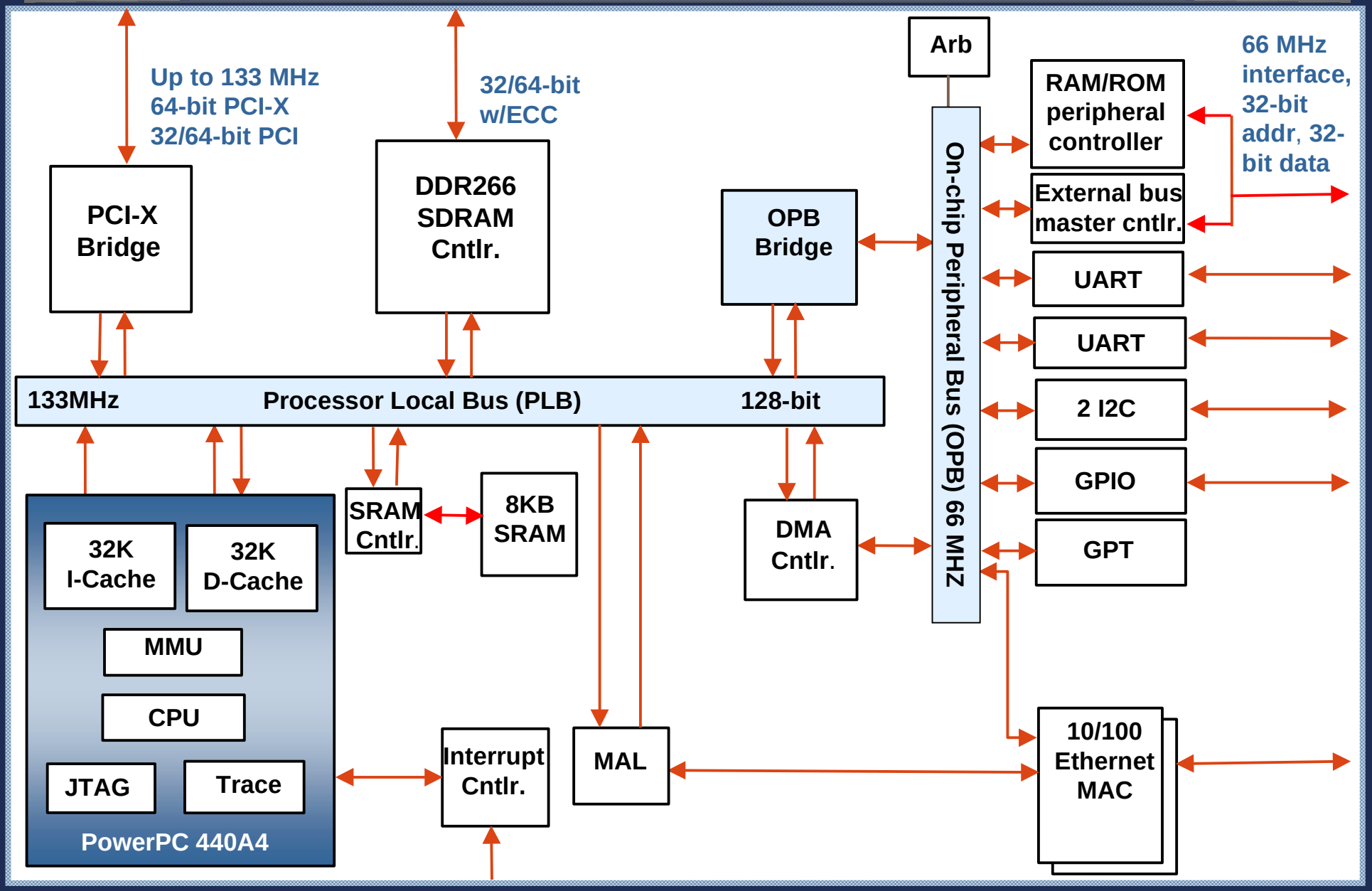
PowerPC Embedded ProcessorRoadmap



Future availability dates are subject to change without notice

440GP Block Diagram



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440GP Architectural Features

- **PowerPC Book E compliant**
  - enables flexible implementations
  - provides enhancements specifically for embedded applications
  - retains PowerPC compatibility - Application code written for other IBM PowerPC processors will run unchanged on the 440GP
- **DCR bus initializes and extracts info from I/O devices in a uniform manner**
- **Cache modes - normal, transient, locked**
- **Address translation enabled at all times**

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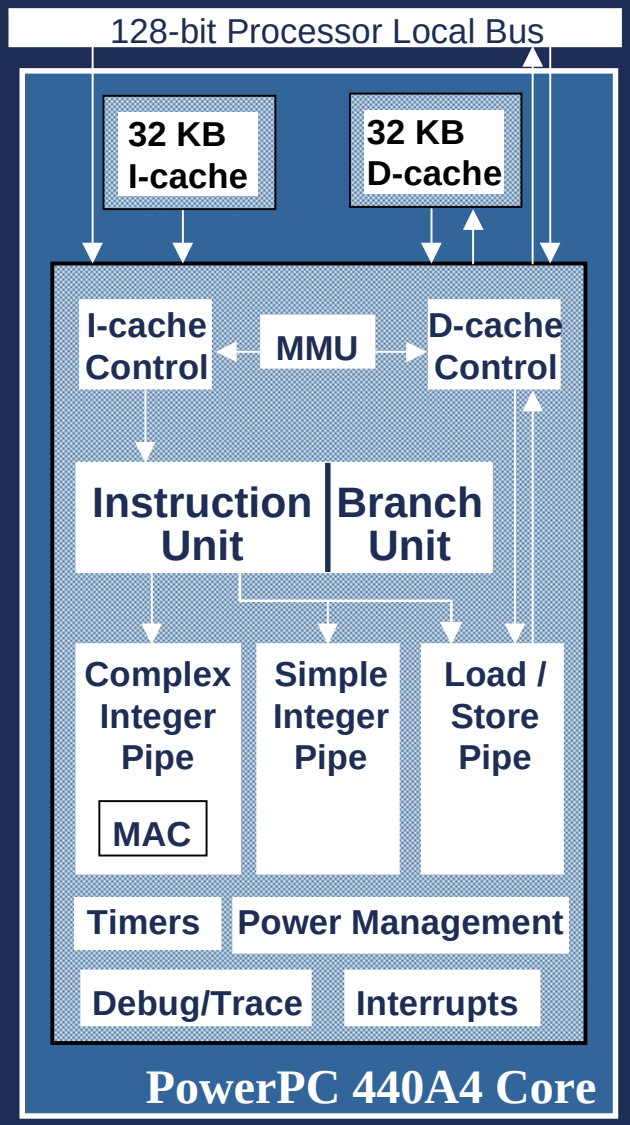
440GP Processor Core Features

- **Superscalar: Two instructions per cycle, out of order execution**
- **7 stage pipeline**
- **Caches**
  - 32KB instruction & 32KB data cache
  - 64-way set associative, 32 byte line
- **Dynamic branch prediction: 16- entry BTAC, 4K- entry BHT, Gshare algorithm**
- **Interrupt controller supports 12 external and 20 internal interrupts**
- **36-bit real address**
- **64-entry, unified, fully associative TLB**
  - 4-entry instruction µTLB
  - 8-entry data µTLB



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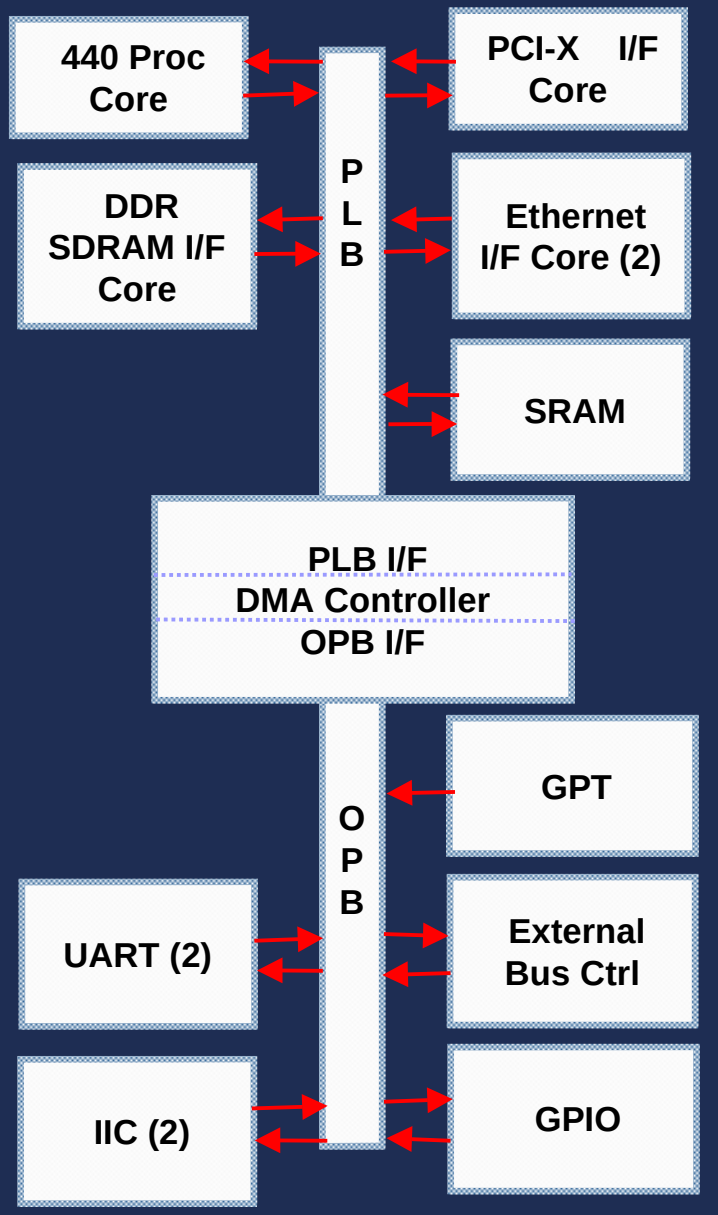
128-bit CoreConnect Bus Architecture

- **Processor Local Bus:**
  - separate and simultaneous read and write 128-bit data paths
  - 36-bit address
  - simultaneous address and data phases
  - 133MHz, maximum 4.2GB/ s
  - processor/bus ratios of 2.5, 3, 3.5, 4
- **On-Chip Peripheral Bus:**
  - dynamic bus sizing 32-, 16-, 8- bit
  - 36-bit address
  - 66MHz, maximum 266MB/ s



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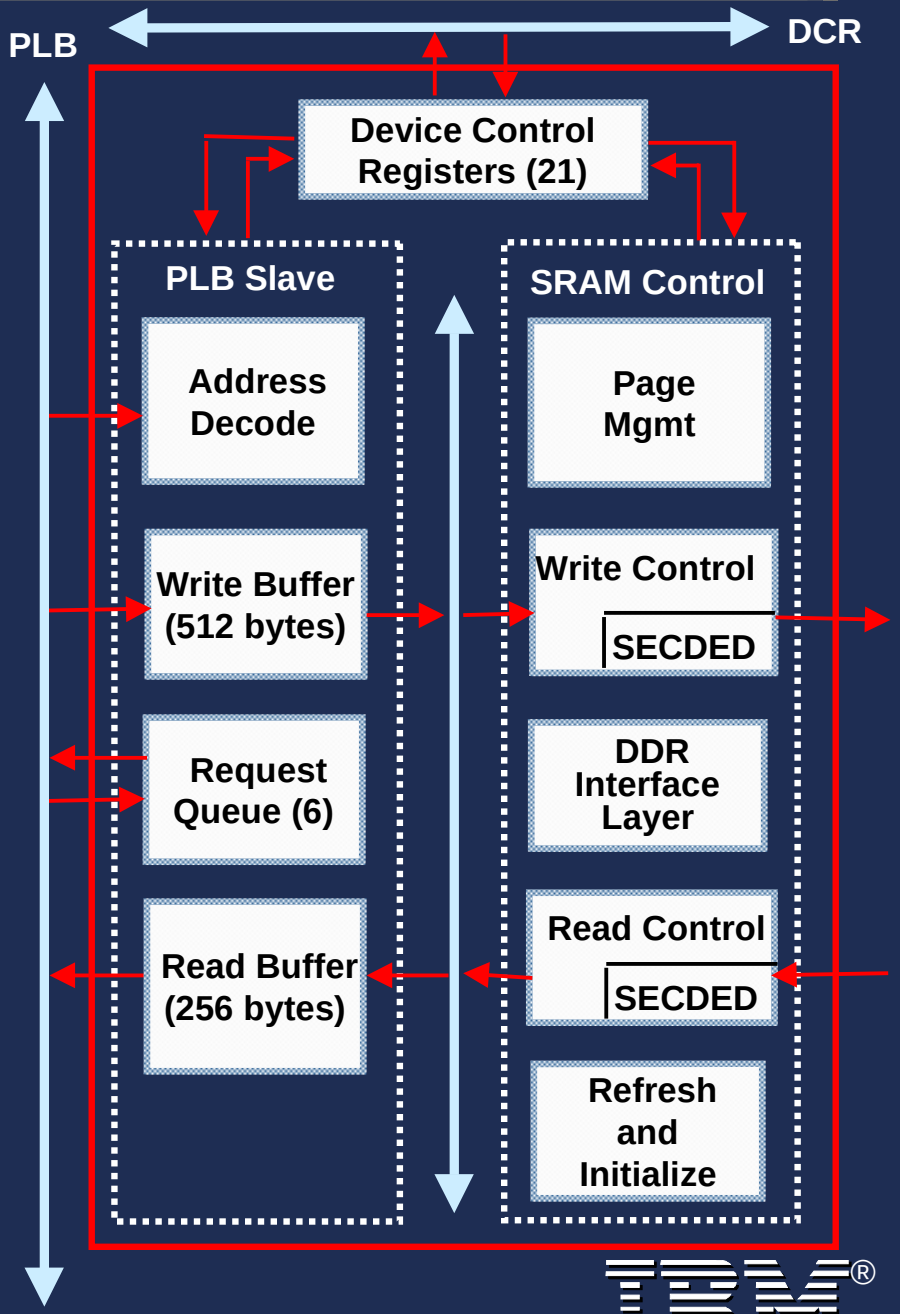
DDR SDRAM Memory Controller

- Supports industry standard DIMMs
- JEDEC PC200/266 compliant
- Maximum of 2GB addressability
- 32-bit or 64-bit memory interface with optional 8-bit ECC (SECDED)
- 2.1 GB/s peak bandwidth at 133 MHz
- Page mode accesses (up to 8 open pages) with configurable paging
- Programmable address mapping and timing
- H/W or S/W initiated self-refresh



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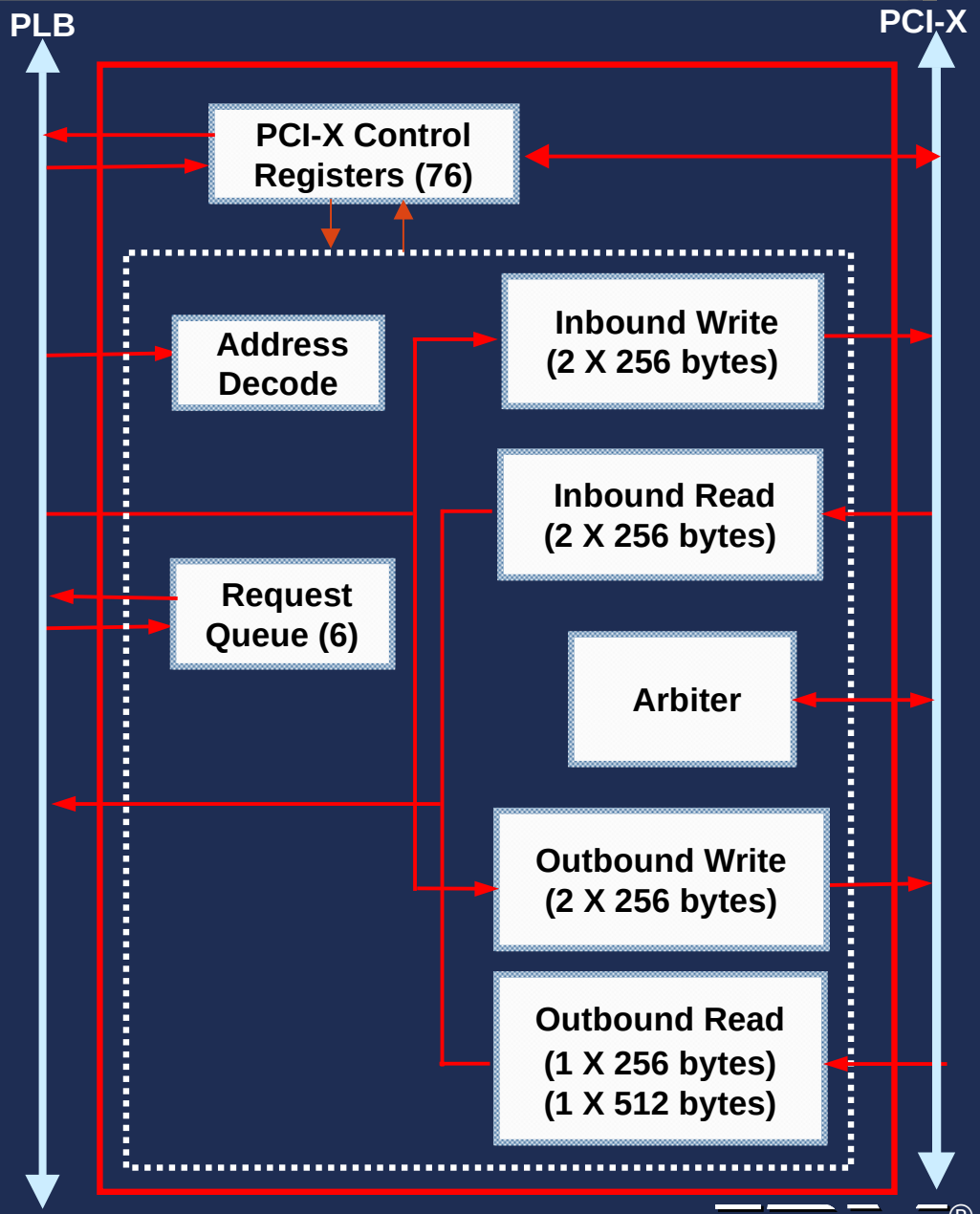
PCI-X Interface

- **PCI-X V1.0 and PCI V2.2**
  - split transactions
  - PCI-X frequency to 133MHz
  - asynchronous with PLB
  - latch-to-latch transfers
  - PCI frequency to 66MHz
- **PCI register set addressable from on-chip processor and PCI device sides**
- **Boot from PCI bus memory**
- **Message Signaled Interrupt support**



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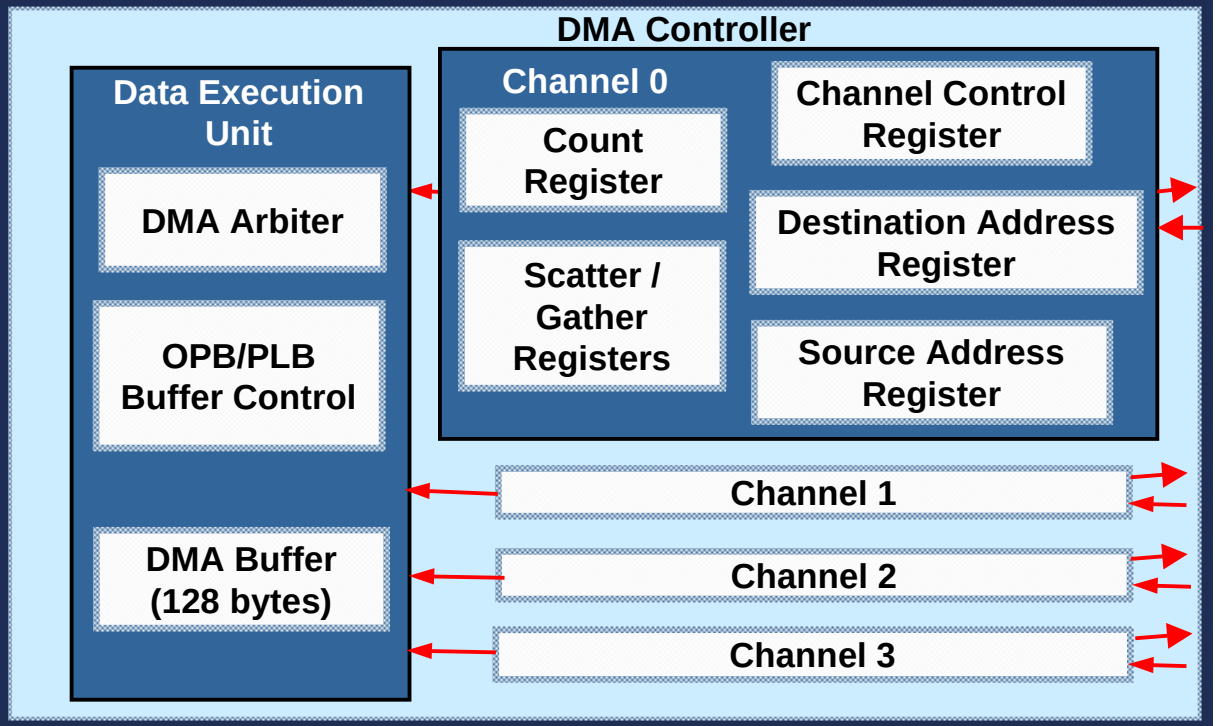
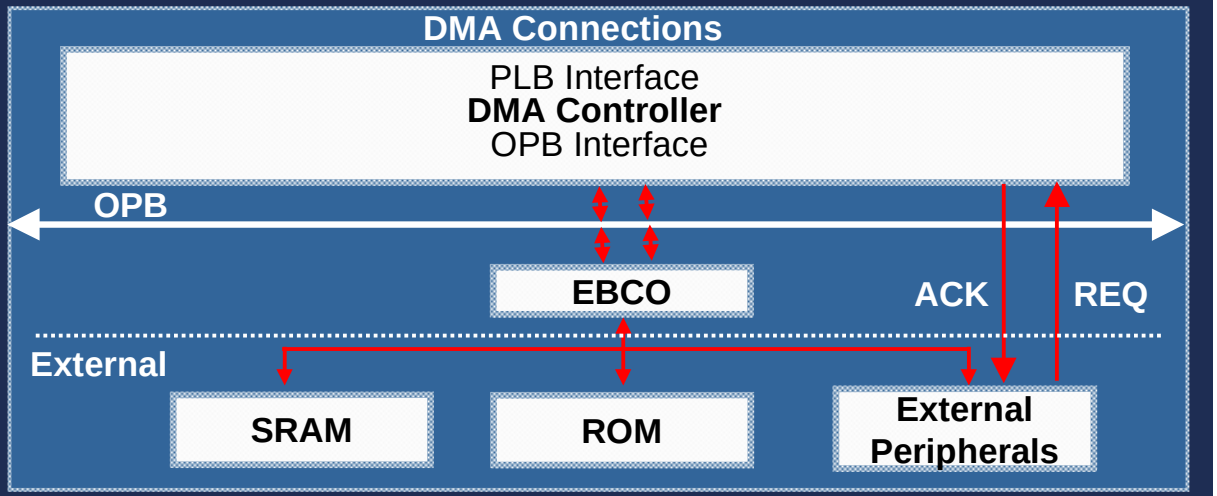
External Bus Controller

- **Four DMA Channels**
  - scatter/gather
  - address increment or decrement
- **8-, 16-, 32-bit external data bus width**
- **Separate 32-bit address bus**
- **External master interface**
- **8 chip selects for external peripherals**
- **Burst and non-burst devices**





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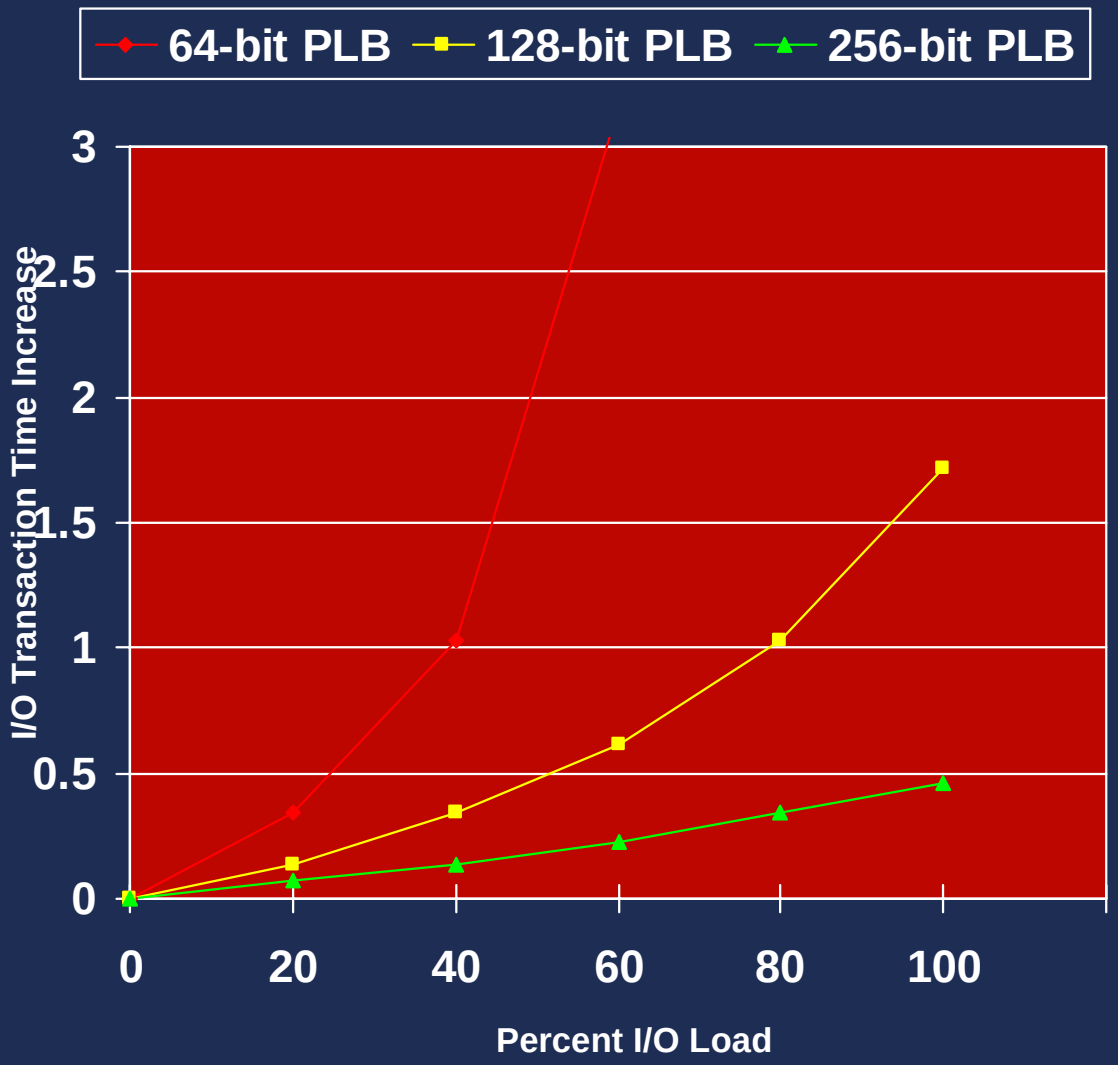
On-Chip Bandwidth Optimization

- **Performance**
  - processor: 720DMIPS (at 400MHz)
  - DDR SDRAM: 2.1GB/s
  - PCI-X: 1.06GB/s
  - PLB: 4.2GB/s at 128-bits, bottleneck at 64-bits, underutilized at 256-bits
  - OPB: 266MB/s at 32-bits
  - ethernet (2) at 10/100 Mb/s each
- **Buffering and queuing to support these rates**



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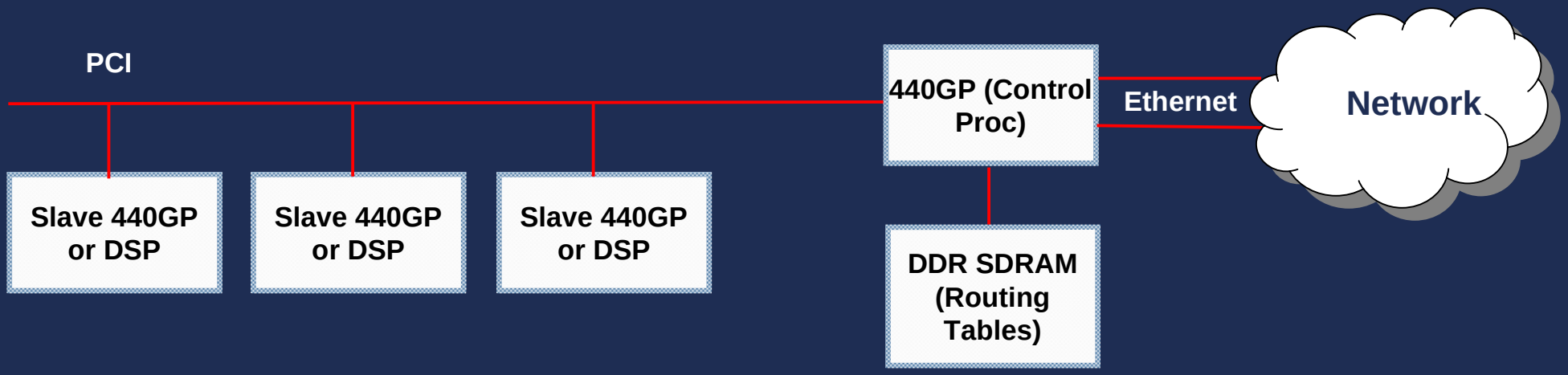
440GP for Wired Communications

- **Processor: host**
- **PCI: network interface, interprocessor communication**
- **Dual Ethernet:**
  - interprocessor communication
  - modem
- **SDRAM: Large storage for routing tables**
- **External Bus:**
  - flash
  - modem
  - ROM
  - DSPs
  - encryption/compression processors



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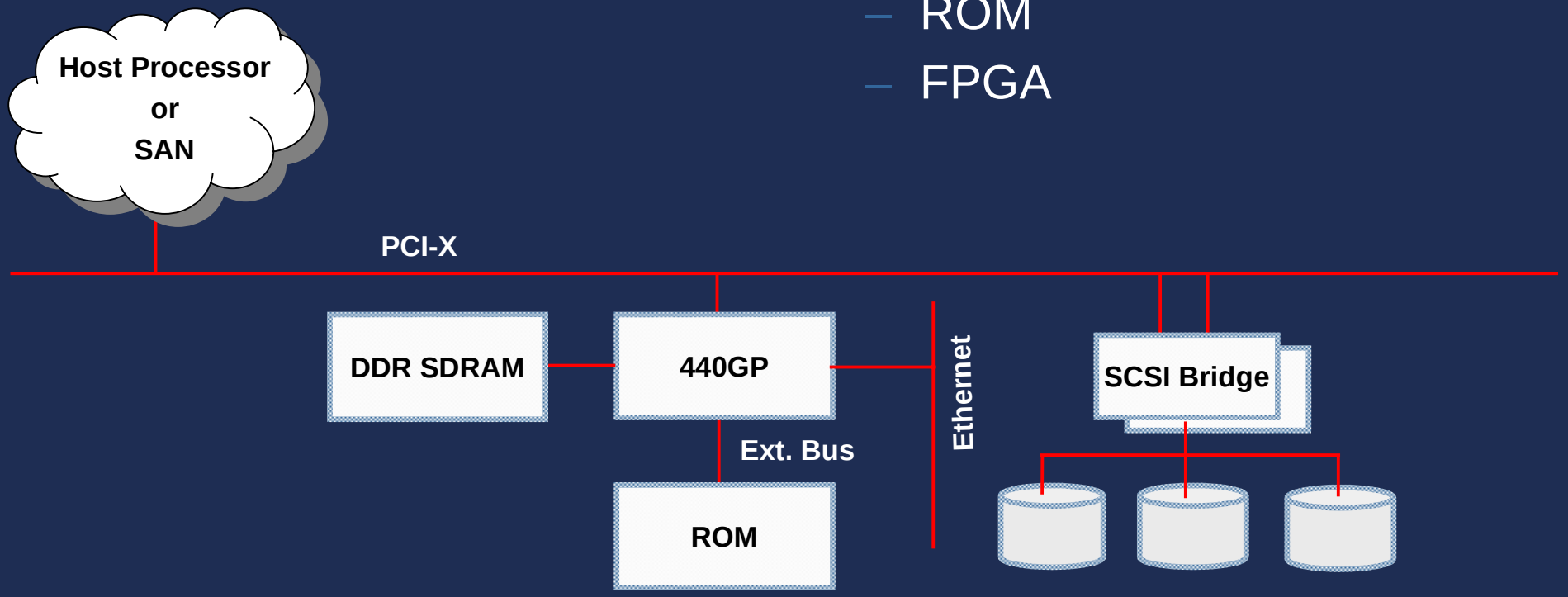
440GP for Storage Applications

- **Processor: Disk Controller**
- **PCI-X:**
  - disk controller (440GP) for Storage Area Network or directly to host
  - bridge to SCSI-3/4 drives
- **Ethernet: system control and RAS**
- **Large SDRAM storage for the following:**
  - disk cache
  - RAID
  - ECC
- **External Bus:**
  - ROM
  - FPGA



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PowerPC 440GP Statistics

Frequency	400 - 500 MHz
Performance (Dhrystone 2.1)	900 DMIPS at 500 MHz
Power Dissipation (est. typical)	< 3 W @ 400 MHz
Architecture	32-bit PowerPC Book E compliant, application code compatible with all IBM PowerPC processors
Die size	59 mm_2
Caches	32/32 KB, 64-way set-associative
Package	552 CBGA, 25 x 25 mm size, 1.0 mm pad pitch, 416 signal I/Os
Technology	0.18 μm (0.11μm L_{eff}) CMOS SA-27E copper, 5 metal layers
Voltage	1.8 V logic, 2.5 V SDRAM I/Os, 3.3 V other I/Os

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Summary

"Beauty may be in the eye of the beholder but performance you can measure."

Thank you!

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